Fast Thyristor
AT358S

Key Parameters

$I_{TAV(M)}$	=	358	A
V_{DRM}/V_{RRM}	=	600 - 1200	V
I_{TSM}	=	5100	A
V_{T0}	=	1.25	V
r_T	=	1	mΩ

Properties

- International standard package
- Metal case with ceramic insulator
- Low on-state and switching losses
- High operation reliability
- Optimum power handling capability

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters			Maximum Limits			Unit
V_{DRM} V_{RRM}	Repetitive peak forward voltage Repetitive peak reverse voltage	t_{vj} = -40 °C ... $t_{vj\ max}$	600 1000		800 1200	V V
V_{DSM}	Non-repetitive peak forward off-state voltage	t_{vj} = -40 °C ... $t_{vj\ max}$	600 1000		800 1200	V V
V_{RSM}	Non-repetitive peak reverse voltage	t_{vj} = +25 °C ... $t_{vj\ max}$	700 1100		900 1300	V V
I_{TAVM}	Average on-state current	t_C = 85 °C t_C = 57 °C	358 510			A A
I_{TRMSM}	RMS on-state current		800			A
I_{TSM}	Surge current	t_{vj} = 25 °C, t_P = 10 ms t_{vj} = $t_{vj\ max}$, t_P = 10 ms	5800 5100			A A
I^2t	I^2t-value	t_{vj} = 25 °C, t_P = 10 ms t_{vj} = $t_{vj\ max}$, t_P = 10 ms	168 130			kA²s kA²s
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	t_{vj} = $t_{vj\ max}$ V_D = 0.67 V_{DRM}		1)	2)	
			B:	50	50	V/µs
			c*:	500	500	V/µs
			L:	500	50	V/µs
			M*:	1000	500	V/µs
$(di/dt)_{cr}$	Critical rate of rise of on-state current	f = 50 Hz, I_{GM} = 1 A di_G/dt = 1 A/µs $V_D \leq 0.67\ V_{DRM}$	500			A/µs

CHARACTERISTICS

Symbols and parameters			Value			Unit
			min	typ	max	
v_T	On-state voltage	$t_{vj} = t_{vj\ max}$, I_T = 1500 A			2.95	V
$V_{(TO)}$	Threshold voltage	$t_{vj} = t_{vj\ max}$		1.25		V
r_T	Slope resistance	$t_{vj} = t_{vj\ max}$		1		mΩ
I_{GT}	Gate trigger current	t_{vj} = 25 °C, v_D = 12 V			250	mA
V_{GT}	Gate trigger voltage	t_{vj} = 25 °C, v_D = 12 V			2.2	V
I_{GD}	Gate non-trigger current	$t_{vj} = t_{vj\ max}$, v_D = 12 V			10	mA
V_{GD}	Gate non-trigger voltage	$t_{vj} = t_{vj\ max}$, v_D = 0.5 V_{DRM}			0.25	V
I_H	Holding current	t_{vj} = 25 °C, v_D = 12 V R_A = 10 Ω			250	mA
I_L	Latching current	t_{vj} = 25 °C, v_D = 12 V R_{GK} ≥ 10 Ω, I_{GM} = 1 A di_G/dt = 1 A/µs t_g = 20 ps			1	A
i_D, i_R	Forward off-state and reverse current	$t_{vj} = t_{vj\ max}$ $v_D = V_{DRM}$, $v_R = V_{RRM}$			50	mA
t_{gd}	Gate controlled delay time	t_{vj} = 25 °C, I_{GM} = 1 A di_G/dt = 1 A/µs			1.2	µs
t_q	Turn-off time	See Techn. Inf.			C*: 12 D: 15 s: 18 E: 20	µs µs µs µs

THERMAL PARAMETERS

Symbols and parameters			Value	Unit
$R_{th(j-c)}$	Thermal resistance, junction to case	Two-sided cooling, θ = 180° el, sin Two-sided cooling, DC Anode-sided cooling, θ = 180° el, sin Anode-sided cooling, DC Cathode-sided cooling, θ = 180° el, sin Cathode-sided cooling, DC	0.053 0.050 0.088 0.085 0.123 0.120	°C/W
$R_{th(c-h)}$	Thermal resistance, case to heatsink	Two-sided Single-sided	0.01 0.02	°C/W
$t_{vj\ max}$	Maximum junction temperature		+125	°C
$t_{c\ op}$	Operating temperature range		-40 ... +125	°C
t_{stg}	Storage temperature range		-40 ... +140	°C

MECHANICAL PARAMETERS

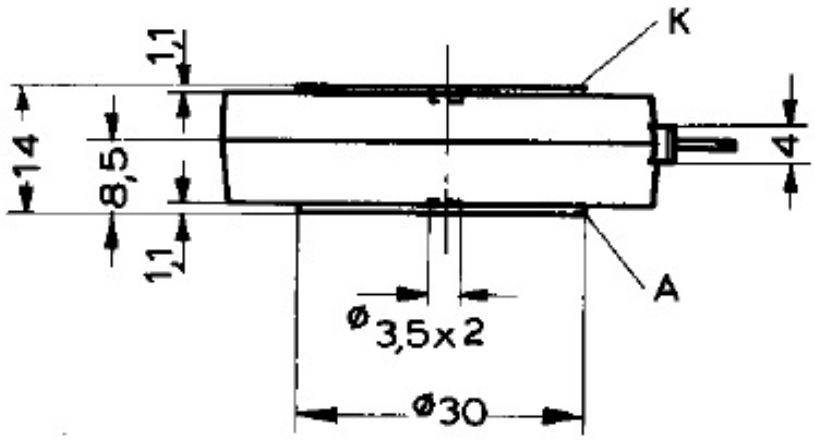
Symbols and parameters			Value	Unit
F	Clamping force		4.5 – 9	kN
W	Weight		110	g
D	Creepage distance		17	mm
a	Vibration resistance	f = 50 Hz	50	m/s^2

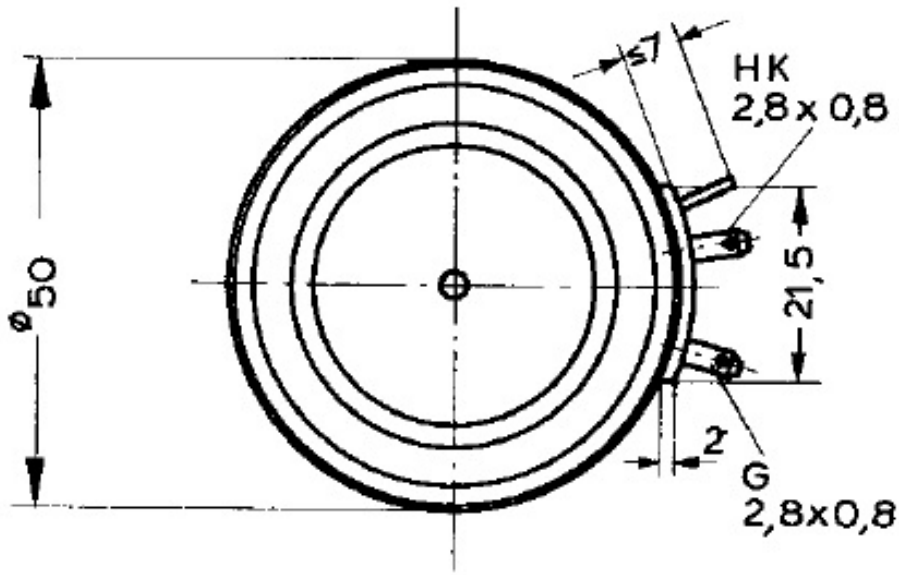
***** - Delivery for larger quantities on request

[1)] - Values to DIN IEC 747-6 (without prior commutation)

[2)] - Immediately after circuit commutated turn-off time, see Parameters t_q

DIMENSIONS





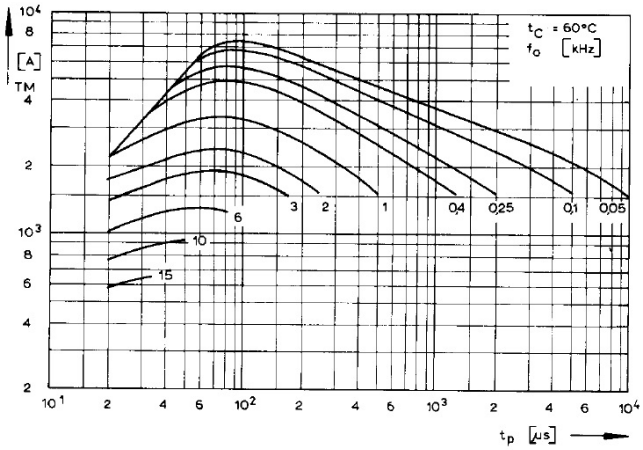


Fig. 1

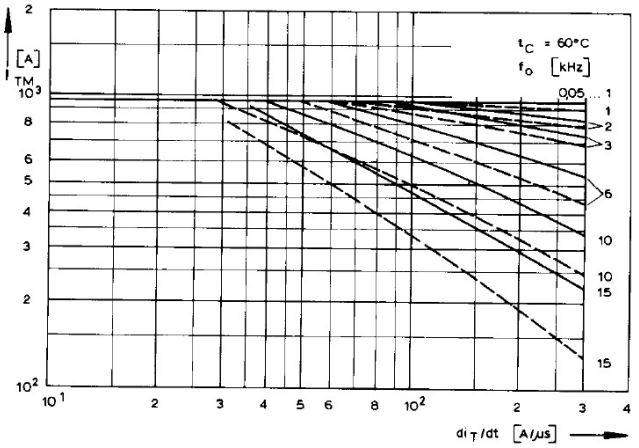


Fig. 4

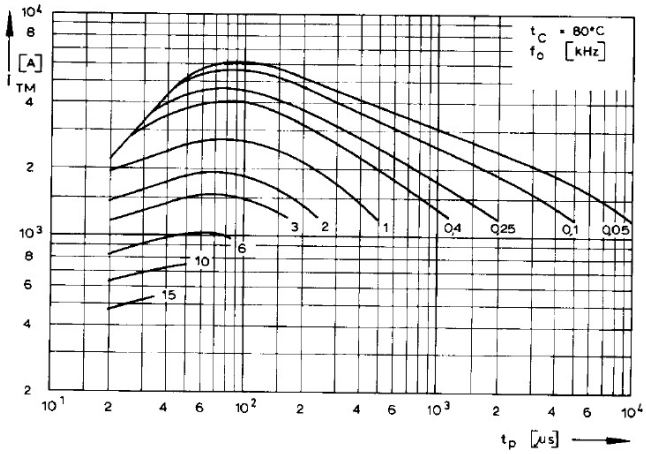


Fig. 2

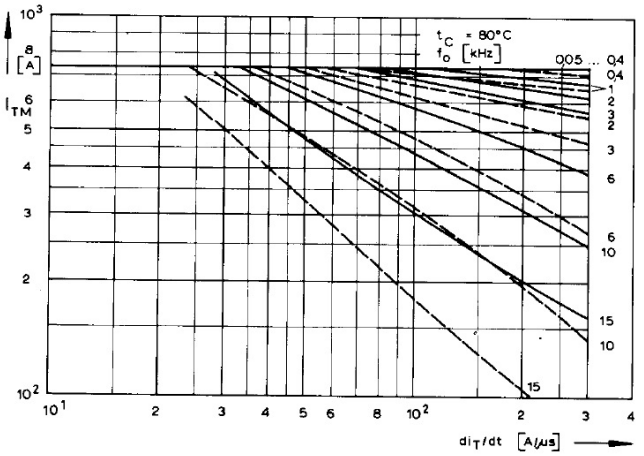


Fig. 5

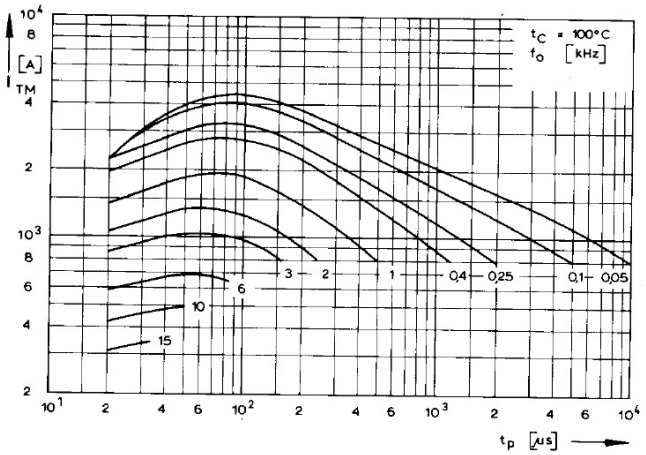


Fig. 3

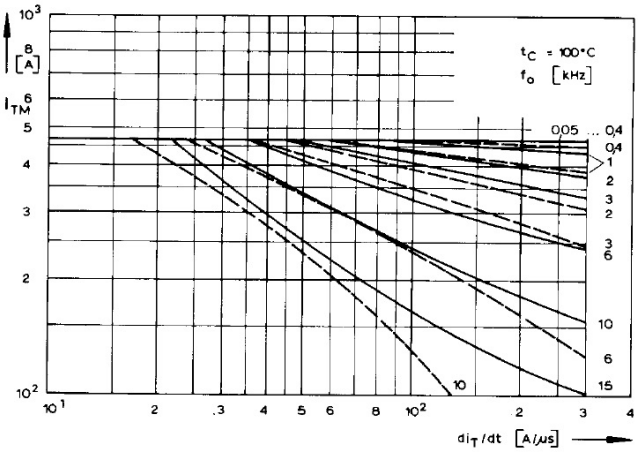


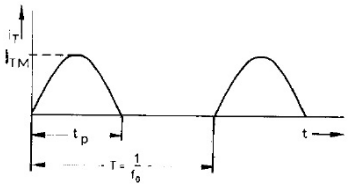
Fig. 6

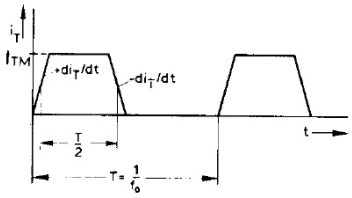
Fig. 1, 2, 3
Pulse generator:
i_G = 1 A, di_G/dt = 1 A/µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.22 µF
v_{DM} ≤ 0.67 V_{DRM}

Fig. 4, 5, 6
Pulse generator:
i_G = 1 A, di_G/dt = 1 A/µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.33 µF
v_{DM} ≤ 0.67 V_{DRM}
dv_R/dt ≤ 600 V/µs
v_{RM} ≤ 0.67 V_{RRM}





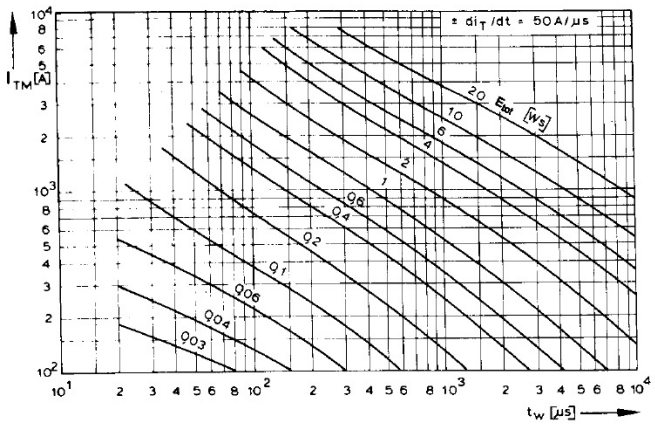


Fig. 7

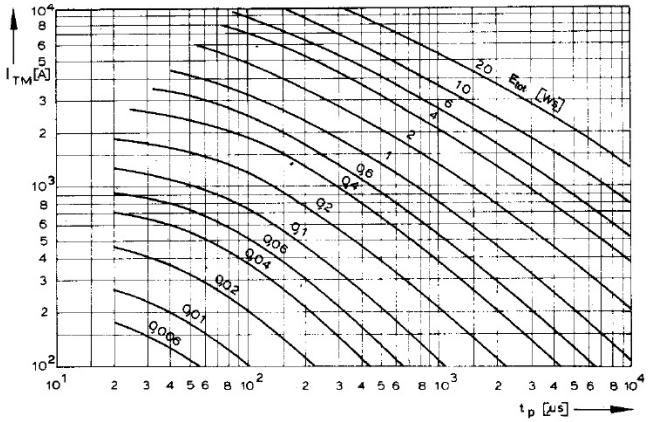


Fig. 10

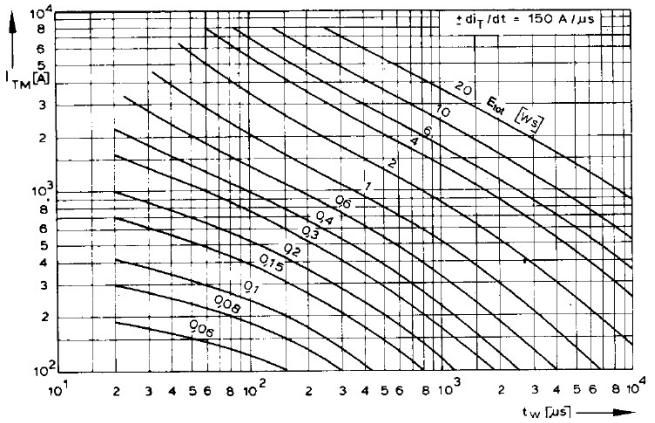


Fig. 8

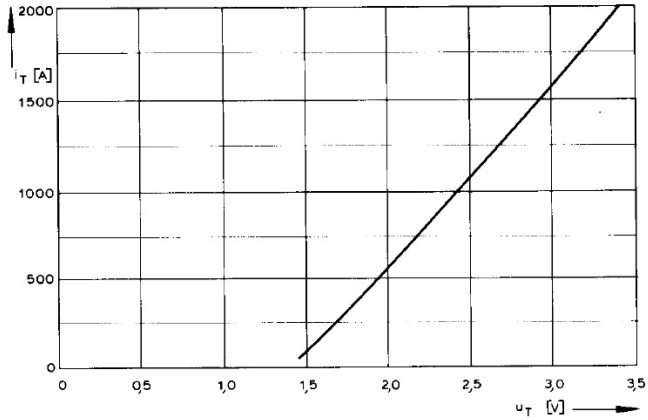


Fig. 11

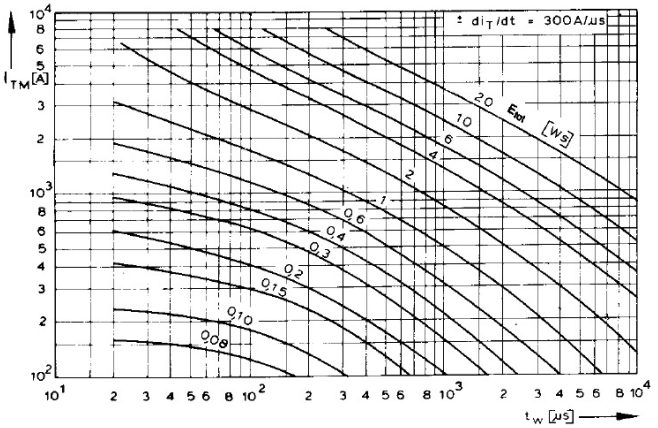


Fig. 9

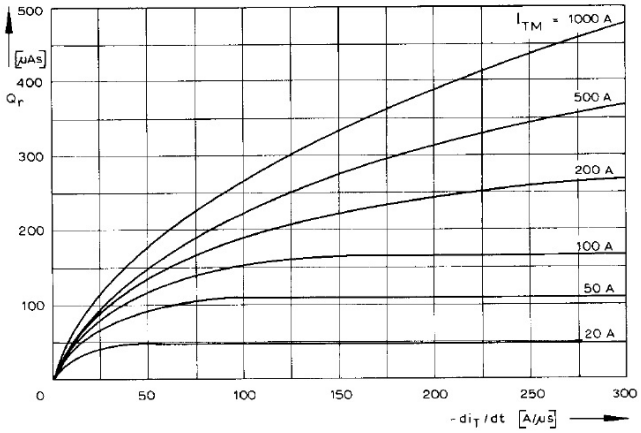


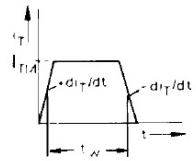
Fig. 12

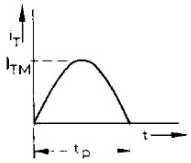
Fig. 7, 8, 9
Pulse generator:
i_G = 1 A, di_G/dt = 1 A/µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.33 µF
v_{DM} ≤ 0.67 V_{DRM}
dv_R/dt ≤ 600 V/µs
v_{RM} ≤ 0.67 V_{RRM}

Fig. 10
Pulse generator:
i_G = 1 A, di_G/dt = 1 A/µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.22 µF





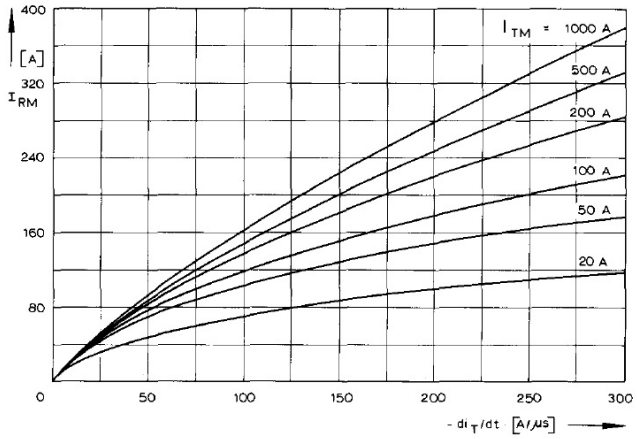


Fig. 13
Peak reverse recovery current
I_{RM} = f(-di/dt), t_{vj} = $t_{vj\ (max)}$, v_R = 0.5 V_{RRM}, v_{RM} = 0.8 V_{RRM}
Parameter: On-state current I_{TM}

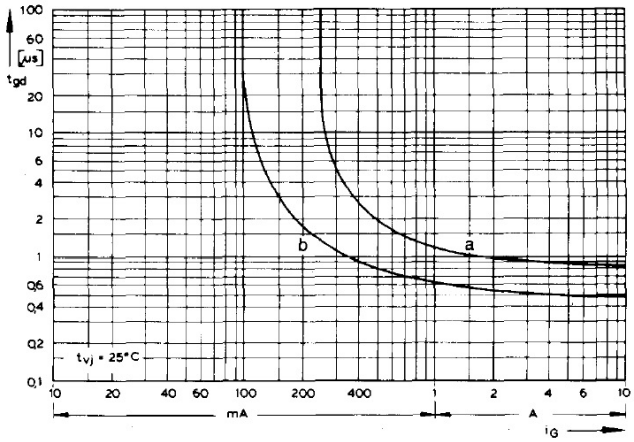


Fig. 15
Gate controlled delay time
t_{gd} = f(i_{GM}), t_{vj} = 25 °C, di_G/dt = i_{GM}/1µs
a — Limiting characteristic
b — Typical characteristic

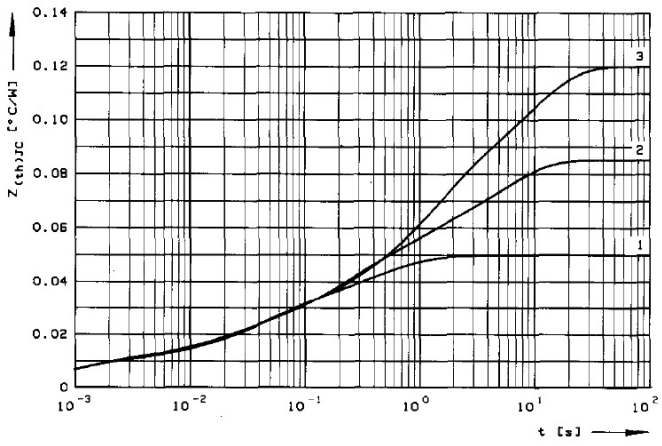


Fig. 14
Transient thermal impedance $Z_{(th)JC}$ = f(t), DC
1 — Two-sided cooling
2 — Anode side cooling
3 — Cathode side cooling

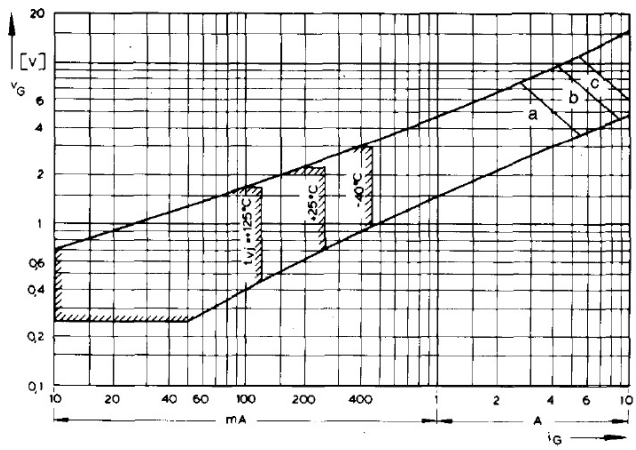


Fig. 16
Gate characteristic with triggering areas v_G = f(i_G), V_D = 12 V
Parameter: Trigger pulse duration t_g [ms]: a - 10; b - 1; c - 0.5
Maximum rated peak gate power dissipation P_{GM} [W]:
a - 20; b - 40; c - 60