Fast Thyristor
AT318F

Key Parameters

$I_{TAV(M)}$	=	318	A
V_{DRM}/V_{RRM}	=	600 - 1300	V
I_{TSM}	=	6000	A
V_{T0}	=	1.3	V
r_T	=	0.7	mΩ

Properties

- International standard package
- Metal case with ceramic insulator
- Low on-state and switching losses
- High operation reliability
- Optimum power handling capability

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters			Maximum Limits			Unit
V_{DRM} V_{RRM}	Repetitive peak forward voltage Repetitive peak reverse voltage		600 1000 1200		800 1100 1300*	V V V
I_{TAVM}	Average on-state current	t_C = 85 °C t_C = 62 °C	318 446			A A
I_{TRMSM}	RMS on-state current		700			A
I_{TSM}	Surge current	t_{vj} = 45 °C, t_P = 10 ms t_{vj} = $t_{vj\ max}$, t_P = 10 ms	6700 6000			A A
I^2t	I^2t-value	t_{vj} = 45 °C, t_P = 10 ms t_{vj} = $t_{vj\ max}$, t_P = 10 ms	224 180			kA^2s kA^2s
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	t_{vj} = $t_{vj\ max}$ V_D = 0.67 V_{DRM}		1)	2)	
			B:	50	50	V/µs
			C*:	400	400	V/µs
			L:	400	50	V/µs
			M*:	1000	400	V/µs
$(di/dt)_{cr}$	Critical rate of rise of on-state current	non rep. rep., I_{TM} = 1.2 kA I_G = 1 A di_G/dt = 1 A/µs	1000 200			A/µs A/µs

CHARACTERISTICS

Symbols and parameters			Value			Unit
			min	typ	max	
v_T	On-state voltage	$t_{vj} = t_{vj\ max}$, I_T = 1.2 kA			2.25	V
$V_{(TO)}$	Threshold voltage	$t_{vj} = t_{vj\ max}$		1.3		V
r_T	Slope resistance	$t_{vj} = t_{vj\ max}$		0.7		mΩ
I_{GT}	Gate trigger current	t_{vj} = 25 °C, v_D = 6 V, R_A = 5 Ω $t_{vj} = t_{vj\ max}$, v_D = 6 V, R_A = 5 Ω			250 10	mA mA
V_{GT}	Gate trigger voltage	t_{vj} = 25 °C, v_D = 6 V, R_A = 5 Ω			2.2	V
I_H	Holding current	t_{vj} = 25 °C, v_D = 6 V, R_A = 5 Ω			250	mA
I_L	Latching current	t_{vj} = 25 °C, v_D = 6 V R_{GK} ≥ 10 Ω, I_G = 1 A di_G/dt = 1 A/µs t_g = 20 µs			1	A
i_D, i_R	Forward off-state and reverse current	$t_{vj} = t_{vj\ max}$ $v_D = V_{DRM}$, $v_R = V_{RRM}$			50	mA
t_{gd}	Gate controlled delay time	I_G = 1 A, di_G/dt = 1 A/µs			1.2	µs
t_q	Turn-off time	See Techn. Inf.			S: 18 E: 20 F: 25	µs µs µs
Q_s	Stored charge	$t_{vj} = t_{vj\ max}$, I_{TM} = 400 A - di_T/dt = 20 A/µs			90	µAs
C_{null}	Null capacitance	t_{vj} = 25 °C, f = 10 kHz			4	nF

THERMAL PARAMETERS

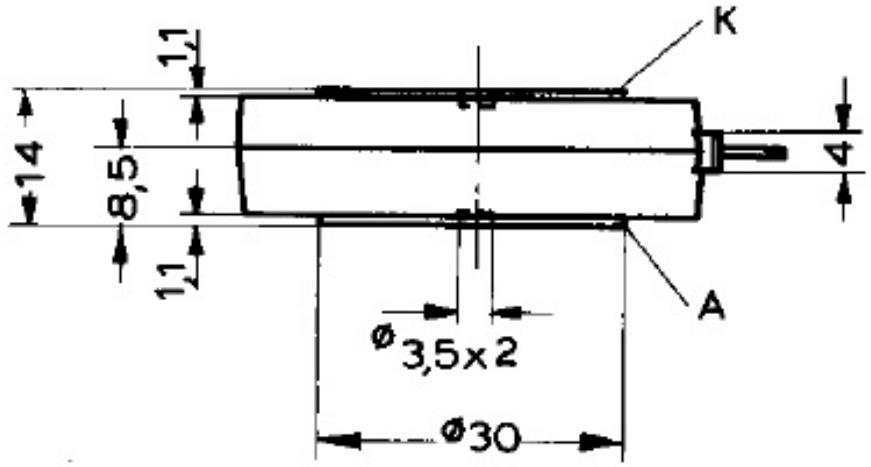
Symbols and parameters			Value	Unit
$R_{th(j-c)}$	Thermal resistance, junction to case	Two-sided cooling, θ = 180° el, sin Two-sided cooling, DC Anode-sided cooling, θ = 180° el, sin Anode-sided cooling, DC Cathode-sided cooling, θ = 180° el, sin Cathode-sided cooling, DC	0.068 0.065 0.113 0.11 0.159 0.156	°C/W
$R_{th(c-h)}$	Thermal resistance, case to heatsink		0.02	°C/W
$t_{vj\ max}$	Maximum junction temperature		+125	°C
$t_{vj\ op}$	Operating temperature range		-40 ... +125	°C
t_{stg}	Storage temperature range		-40 ... +140	°C

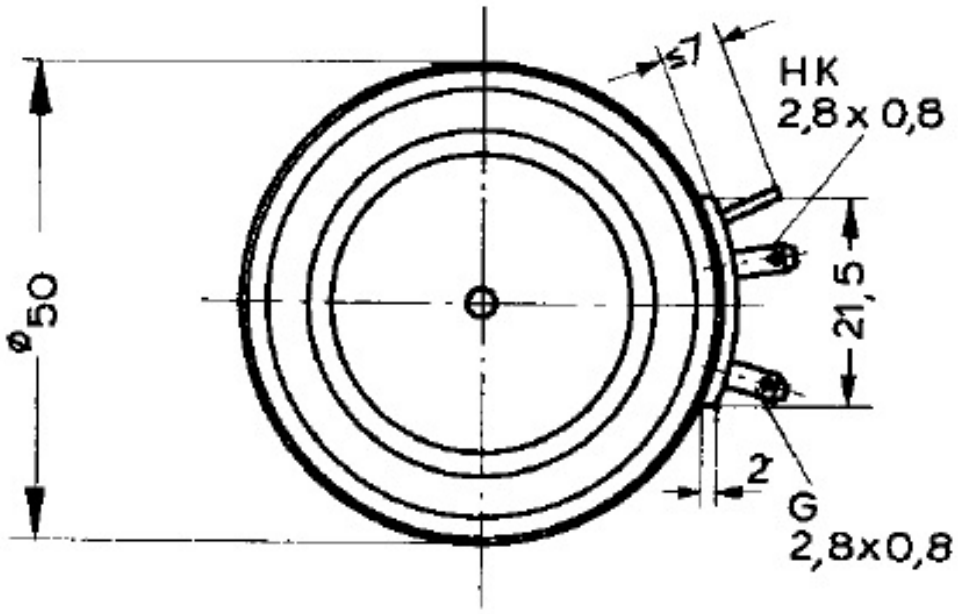
MECHANICAL PARAMETERS

Symbols and parameters			Value	Unit
F	Clamping force		5.5 – 8	kN
W	Weight		110	g
D	Creepage distance		8	mm

***** - Delivery for larger quantities on request
[1)] - Values to DIN IEC 41787 (without prior commutation)
[2)] - Immediately after turn-off time

DIMENSIONS





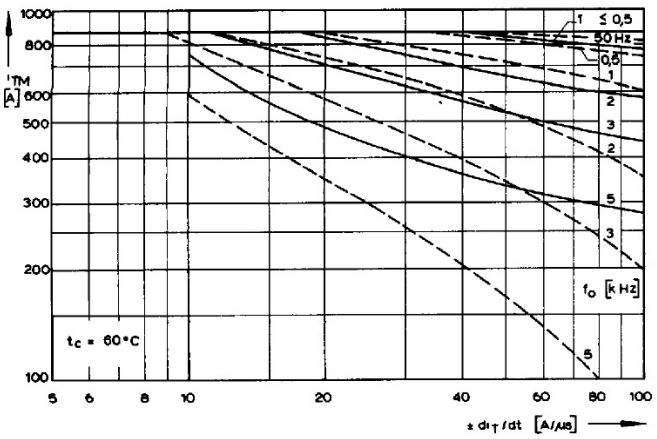


Fig. 1

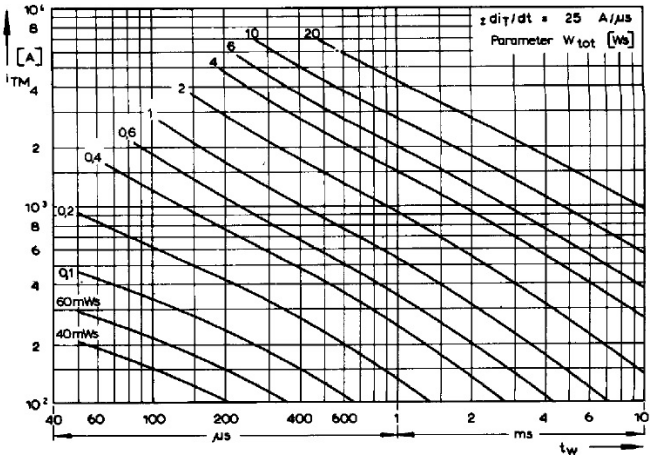


Fig. 4

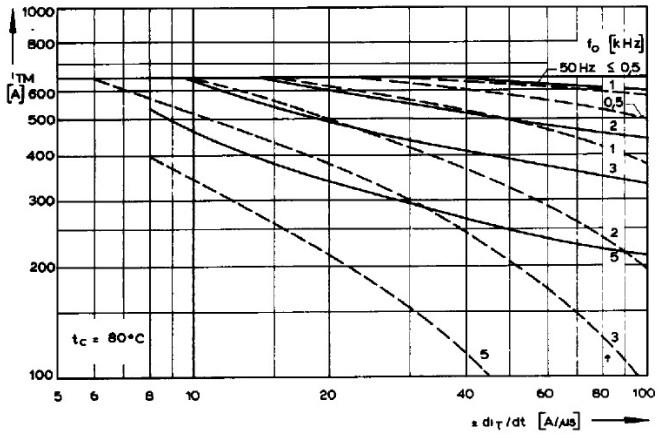


Fig. 2

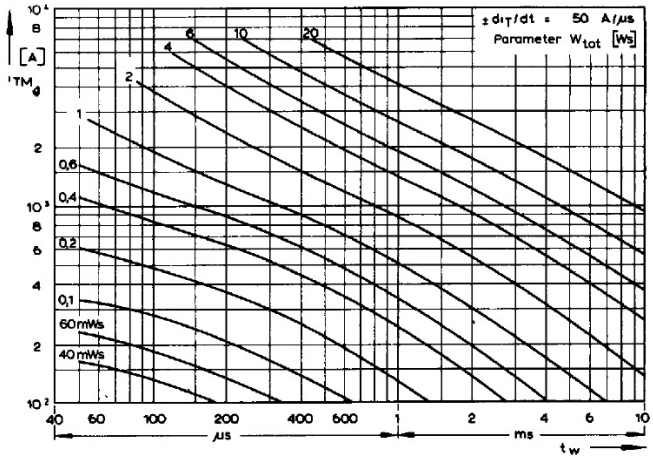


Fig. 5

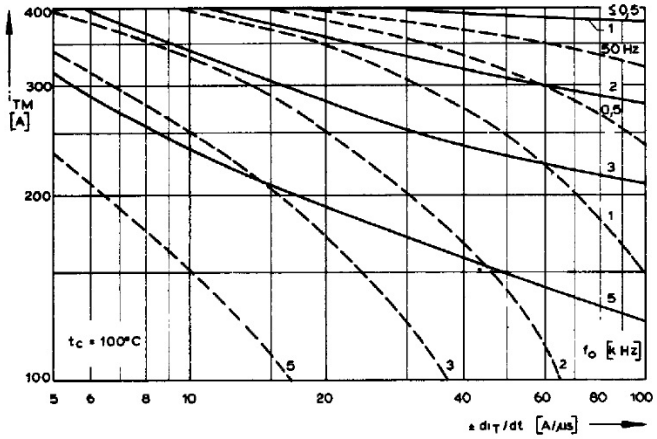


Fig. 3

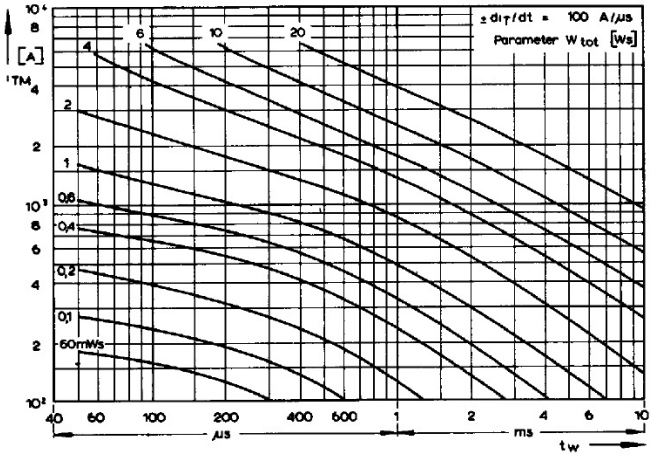
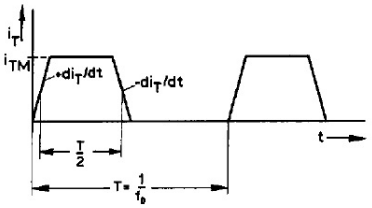


Fig. 6

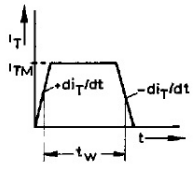
Pulse generator:
i_G = 1 A, t_a = 1 µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.33 µF
dv_R/dt ≤ 600 V/µs



Pulse generator:
i_G = 1 A, t_a = 1 µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.33 µF



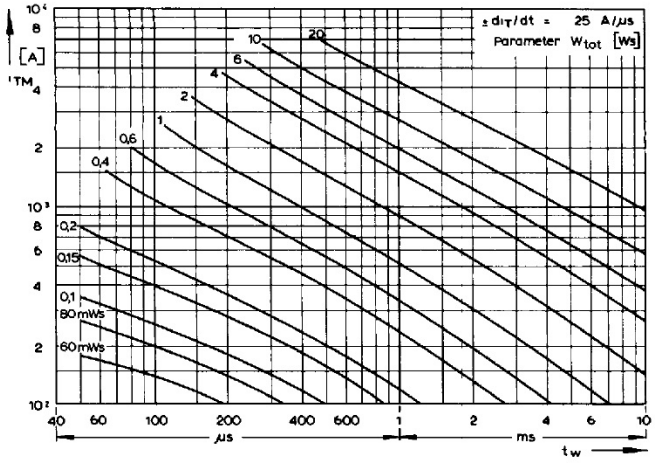


Fig. 7

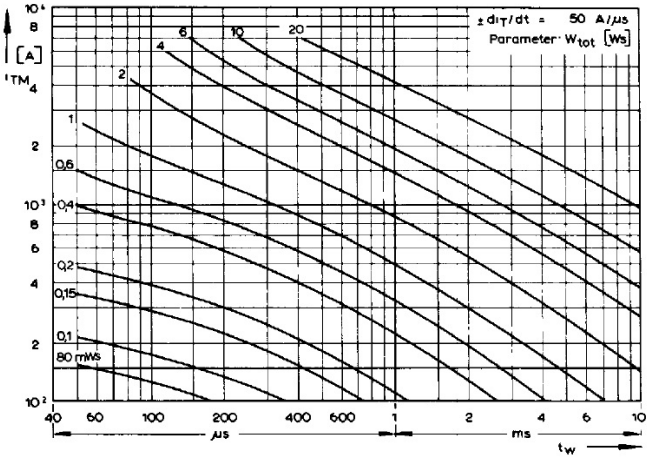


Fig. 8

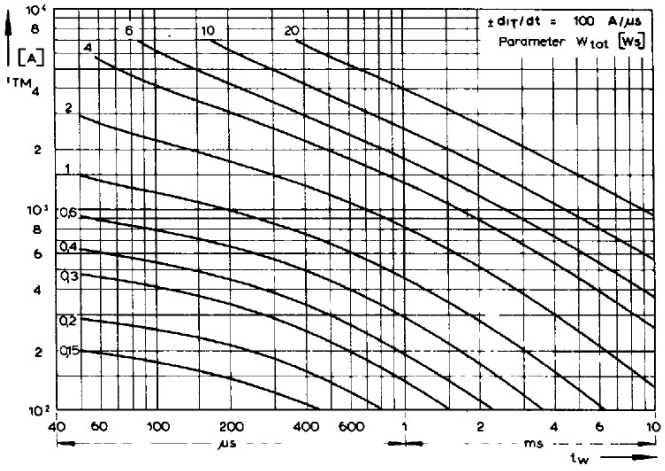


Fig. 9

Pulse generator:
i_G = 1 A, t_a = 1 µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.33 µF
dv_R/dt ≤ 600 V/µs

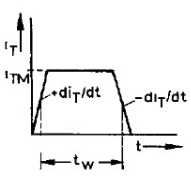


Fig. 10

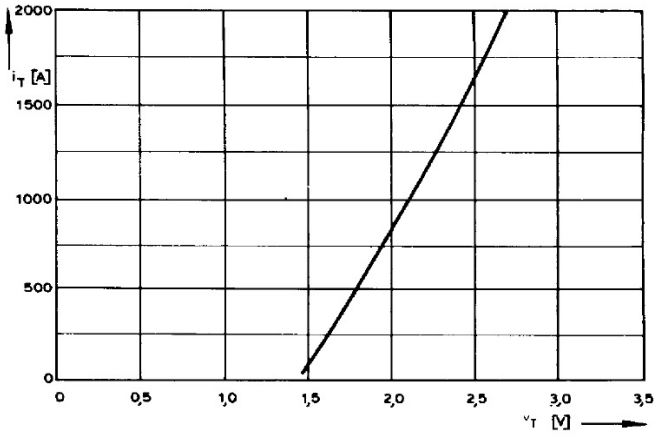


Fig. 11

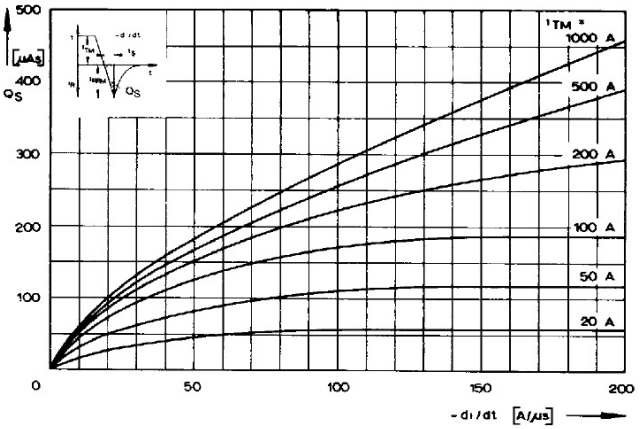
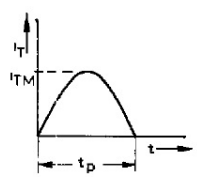


Fig. 12

Fig. 10
Pulse generator:
i_G = 1 A, t_a = 1 µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.22 µF



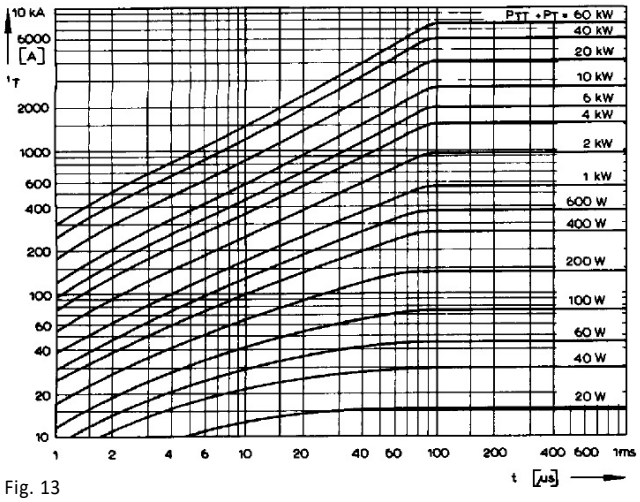


Fig. 13
Diagram for the determination of the sum of the turn-on and forward on-state power loss ($P_{TT}+P_T$).

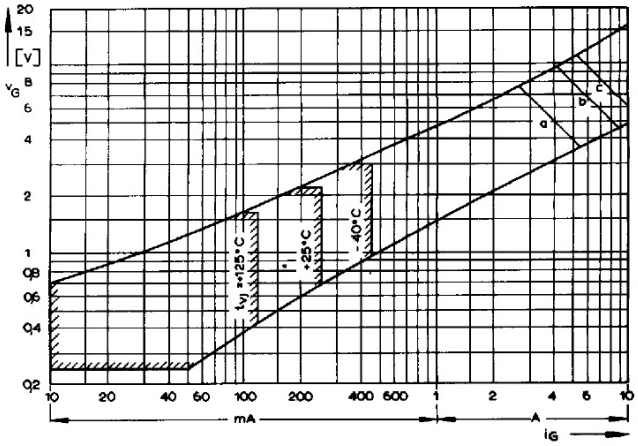


Fig. 16
Gate characteristic and peak gate power dissipation $v_D \geq 6$ V
Parameter: Pulse duration t_g [ms]: a - 10; b - 1; c - 0.5
Maximum allowable peak gate power [W]: a - 20; b - 40; c - 60

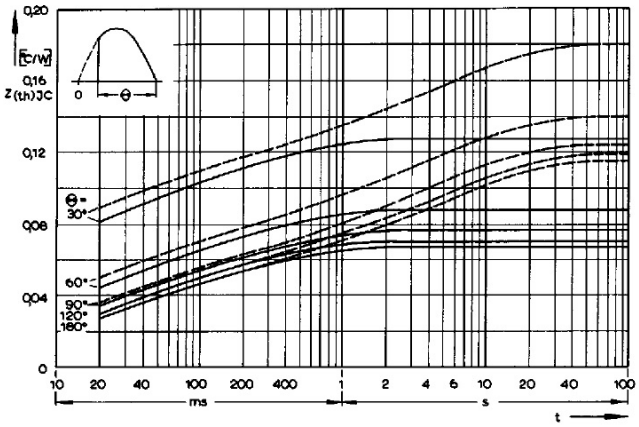


Fig. 14
Transient thermal impedance, junction to case, $Z_{(th)JC}$
- - Anode sided cooling
— Two-sided cooling

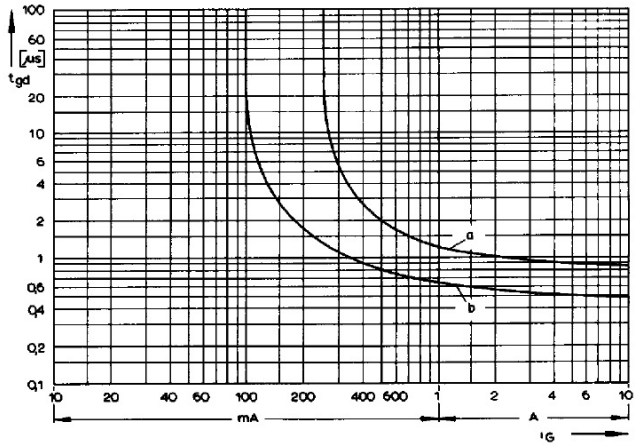


Fig. 17
Gate controlled delay time t_{gd} to DIN 41787 at t_{vj} = 25 °C, t_a = 1 µs
a — Limiting characteristic
b — Typical characteristic

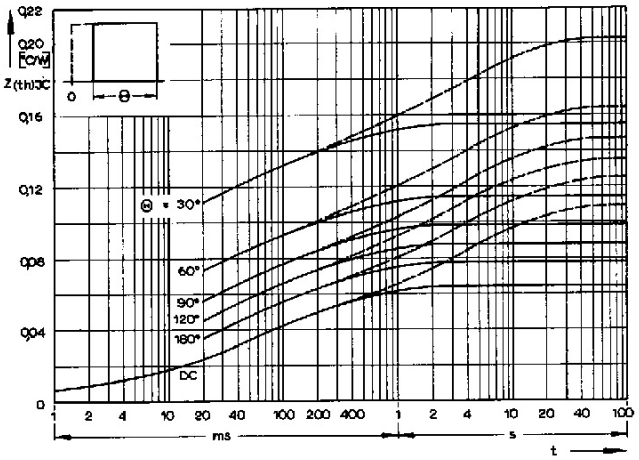


Fig. 15
Transient thermal impedance, junction to case, $Z_{(th)JC}$
- - Anode sided cooling
— Two-sided cooling

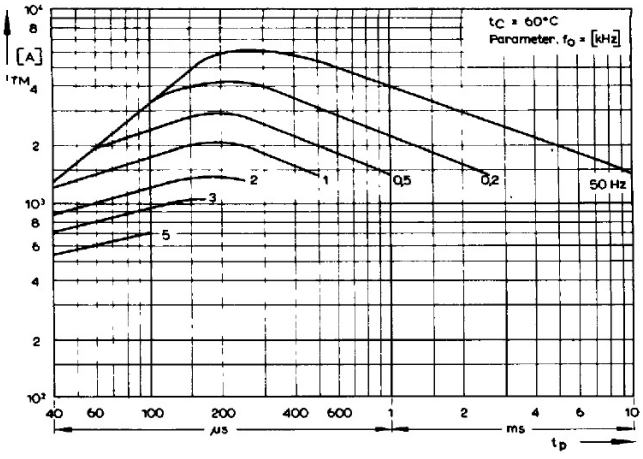


Fig. 18

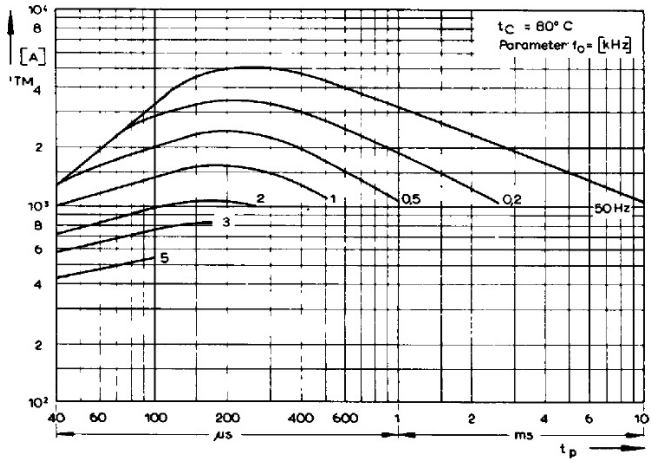


Fig. 19

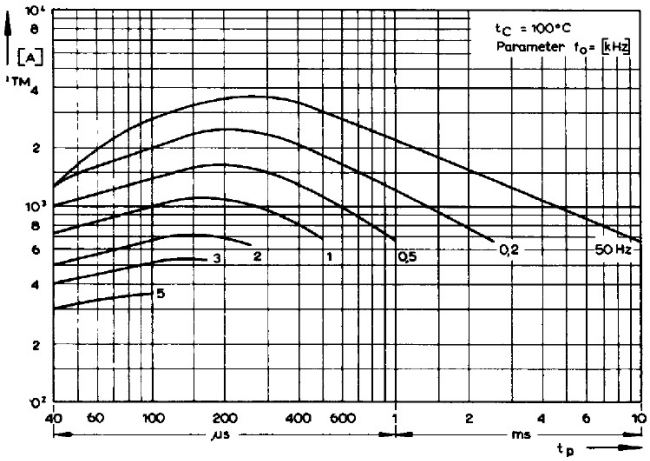


Fig. 20

Pulse generator:
i_G = 1 A, t_a = 1 µs

RC-network:
R [Ω] ≥ 0.02 v_{DM} [V]
C ≤ 0.22 µF
dv_R/dt ≤ 600 V/µs