AS ENERGI

Thyristor Diode Modules
AMKH 215-18E

Symbols and parameters			Values	Units
I_{TAV}	Average on-state current	sin. 180; T_C = 85 (100)°C	215 (153)	A
I_{TSM}	Surge on-state current	T_j = 25°C; 10 ms T_j = 125°C; 10 ms	7000 5700	A A
I^2t	I^2t value, rating for fusing	T_j = 25°C; 10 ms T_j = 125°C; 10 ms	245000 162450	A^2s A^2s
V_{RSM}	Non-repetitive peak reverse voltage		1900	V
V_{RRM} ; V_{DRM}	Repetitive peak reverse voltage; Repetitive peak off-state voltage		1800	V
$(di/dt)_{cr}$	Critical rate of rise of on-state current	T_j = 125°C	200	A/µs
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	T_j = 125°C	1000	V/µs
T_j	Virtual junction temperature		-40 ... +125	°C
T_{stg}	Storage temperature range		-40 ... +125	°C
V_{ISOL}	Insulation test voltage (r.m.s.)	a.c. 50 Hz; r.m.s.; 1s / 1min.	3600 / 3000	V
V_T	On-state voltage	T_j = 25°C; I_T =600 A	max. 1.5	V
$V_{T(TO)}$	On-state threshold voltage	T_j = 125°C	max. 0.85	V
r_T	On-state slope resistance	T_j = 125°C	max. 1.2	mΩ
I_{DD} ; I_{RD}	Forward off-state current; Direct reverse current	T_j = 125°C, V_{RD}=V_{RRM}; V_{DD}=V_{DRM}	max. 60	mA
t_{gd}	Gate controlled turn-on delay time	T_j = 25 °C; I_G = 1 A; di_G/dt = 1 A/µs	1	µs
t_{gr}	Gate controlled rise time	V_D = 0,67 * V_{DRM}	2	µs
t_q	Turn-off time	T_j = 125°C	150	µs
I_H	Holding current	T_j = 25°C; typ. / max	150 / 400	mA
I_L	Latching current	T_j = 25°C; R_G=33Ω; typ. / max	300 / 1000	mA
V_{GT}	Gate trigger voltage	T_j = 25°C; d.c.	min. 2	V
I_{GT}	Gate trigger current	T_j = 25°C; d.c.	min. 150	mA
V_{GD}	Gate non-trigger voltage	T_j = 125°C; d.c.	max. 0.25	V
I_{GD}	Gate non-trigger current	T_j = 125°C; d.c.	max. 10	mA
$R_{th(j-c)}$	Thermal resistance, junction to case	cont. DC; per chip / per module	0.12 / 0.06	K/W
		sin.180; per chip / per module	0.125 / 0.065	K/W
		rec.120; per chip / per module	0.14 / 0.07	K/W
$R_{th(c-s)}$	Thermal resistance, junction to heatsink	per chip / per module	0.04 / 0.027	K/W
M_S	Mounting torque on heatsink	min / max	4.25 / 5.75	Nm
M_t	Mounting torque for terminals	min / max	4.25 / 5.75	Nm
a	Maximum allowable acceleration		5*9.81	m/s^2
W	Weight	approx.	165	g

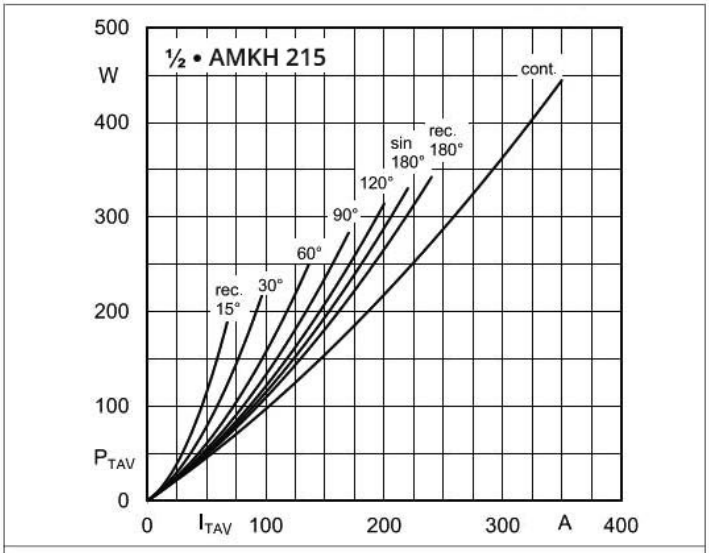


Fig. 1L: Power dissipation per thyristor vs. on-state current

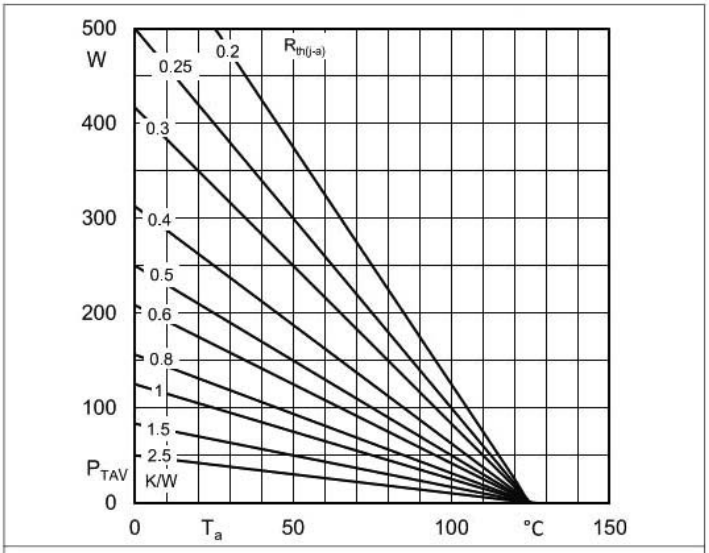


Fig. 1R: Max. power dissipation per chip vs. ambient temperature

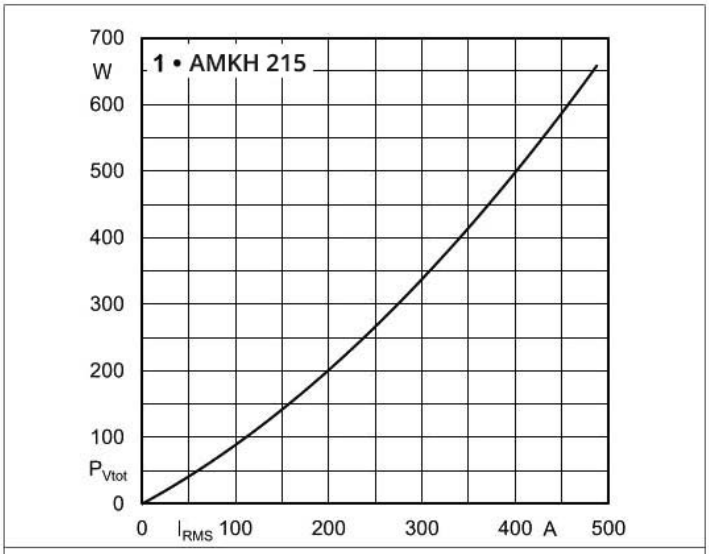


Fig. 2L: Max. power dissipation of one module vs. rms current

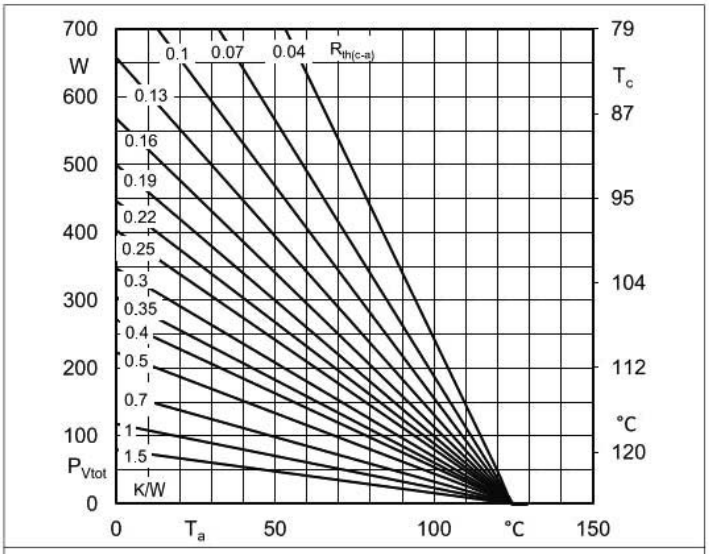


Fig. 2R: Max. power dissipation of one module vs. case temperature

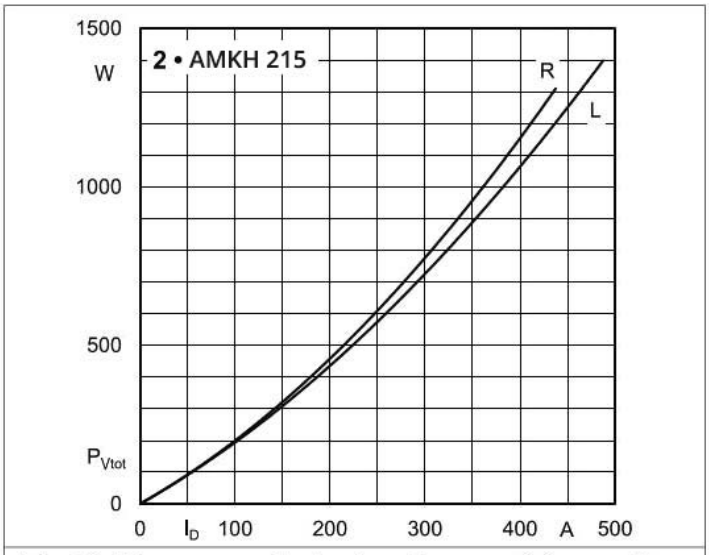


Fig. 3L: Max. power dissipation of two modules vs. direct current

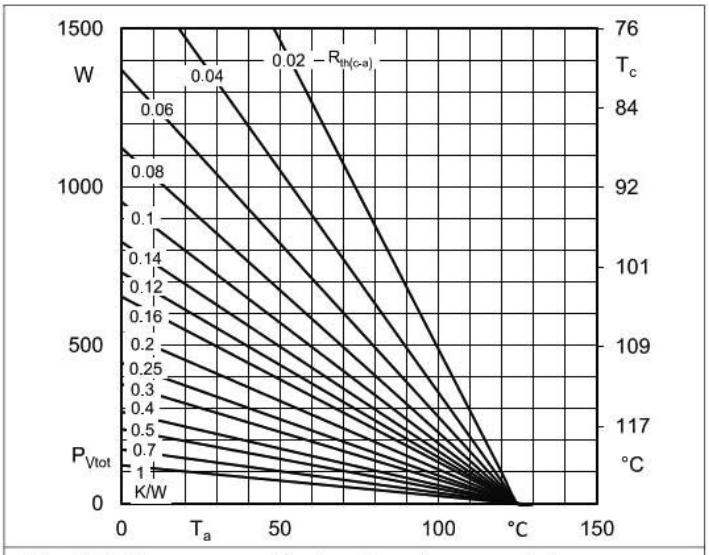


Fig. 3R: Max. power dissipation of two modules vs. case temperature

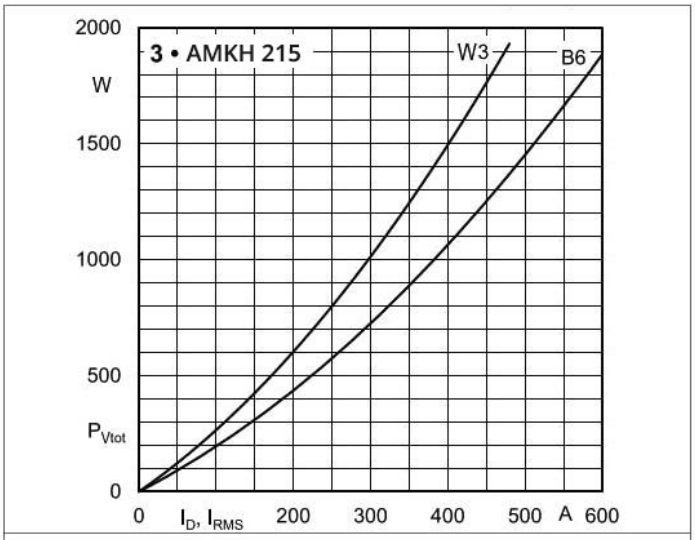


Fig. 4L: Max. power dissipation of three modules vs. direct current

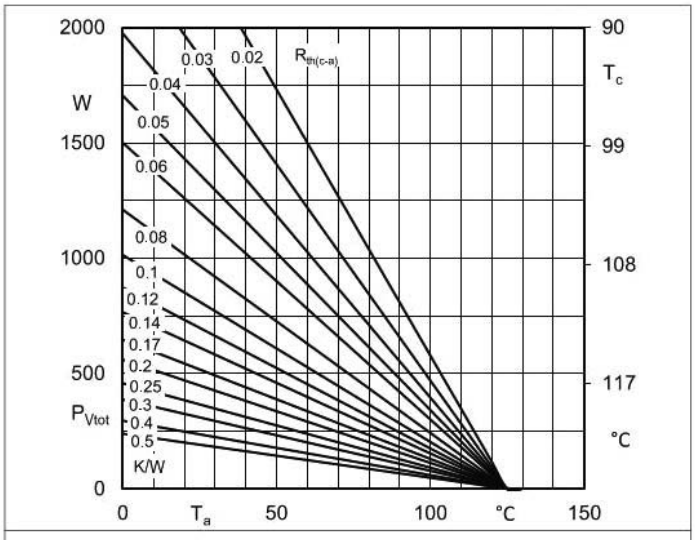


Fig. 4R: Max. power dissipation of three modules vs. case temperature

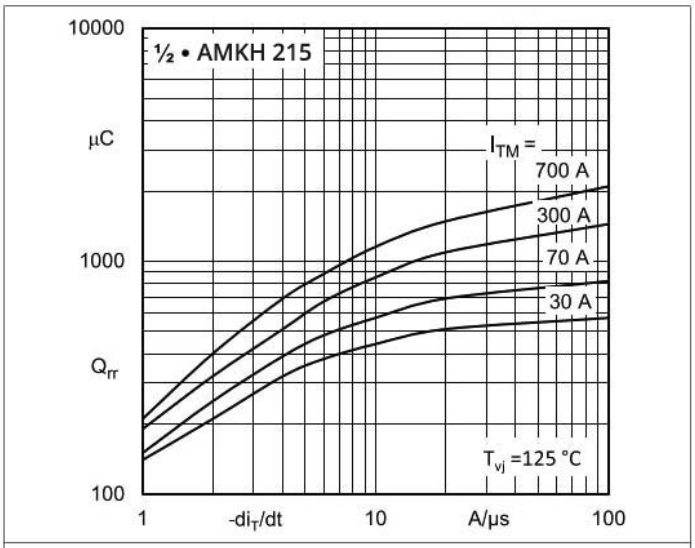


Fig. 5: Recovered charge vs. current decrease

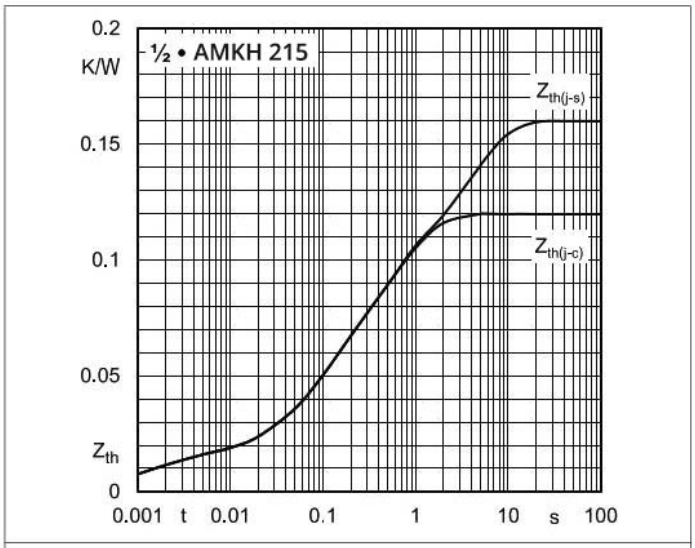


Fig. 6: Transient thermal impedance vs. time

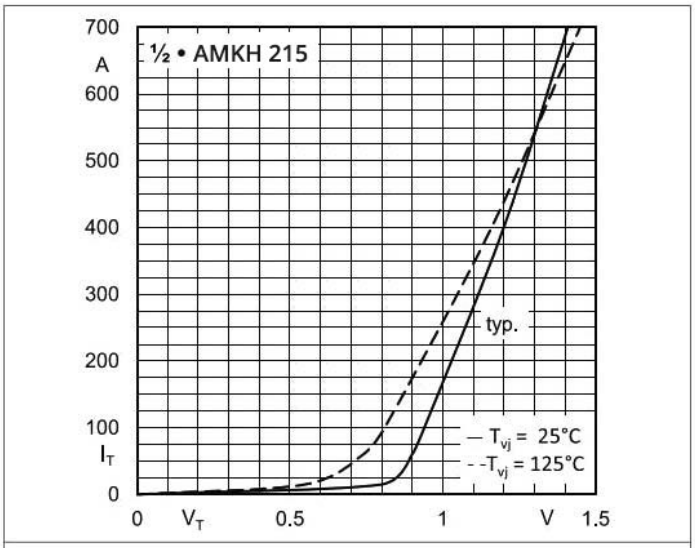


Fig. 7: On-state characteristics

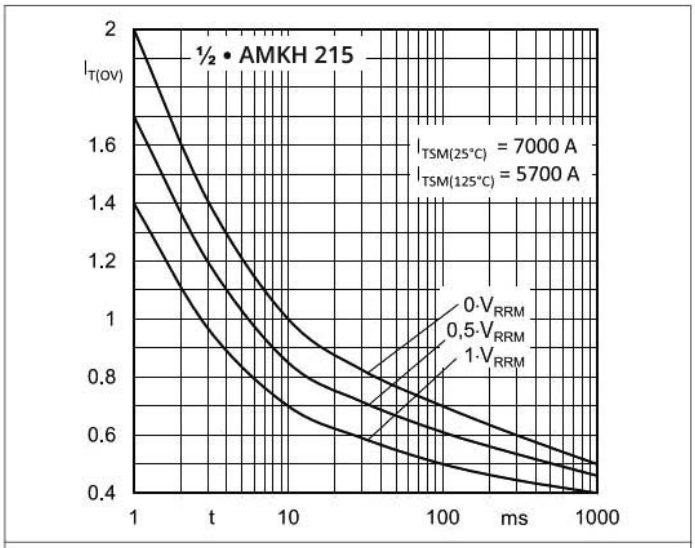


Fig. 8: Surge overload current vs. time

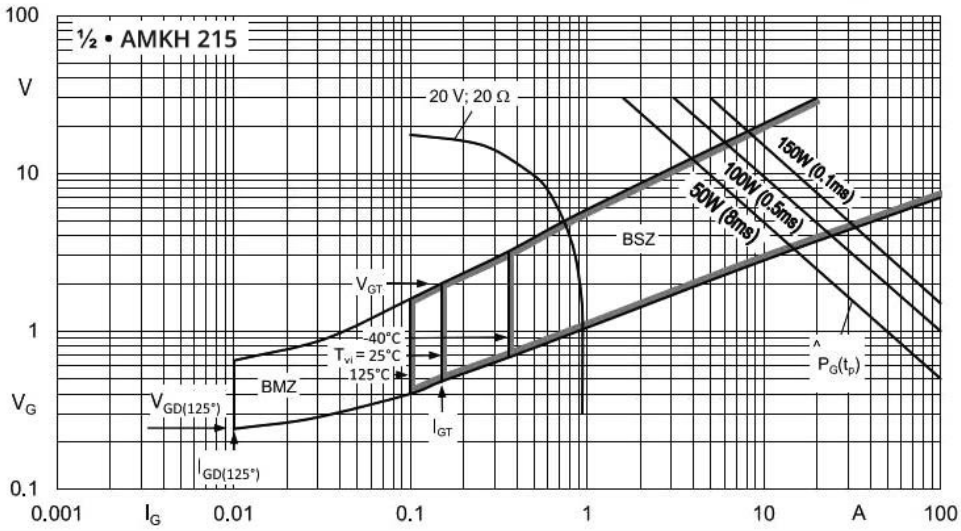
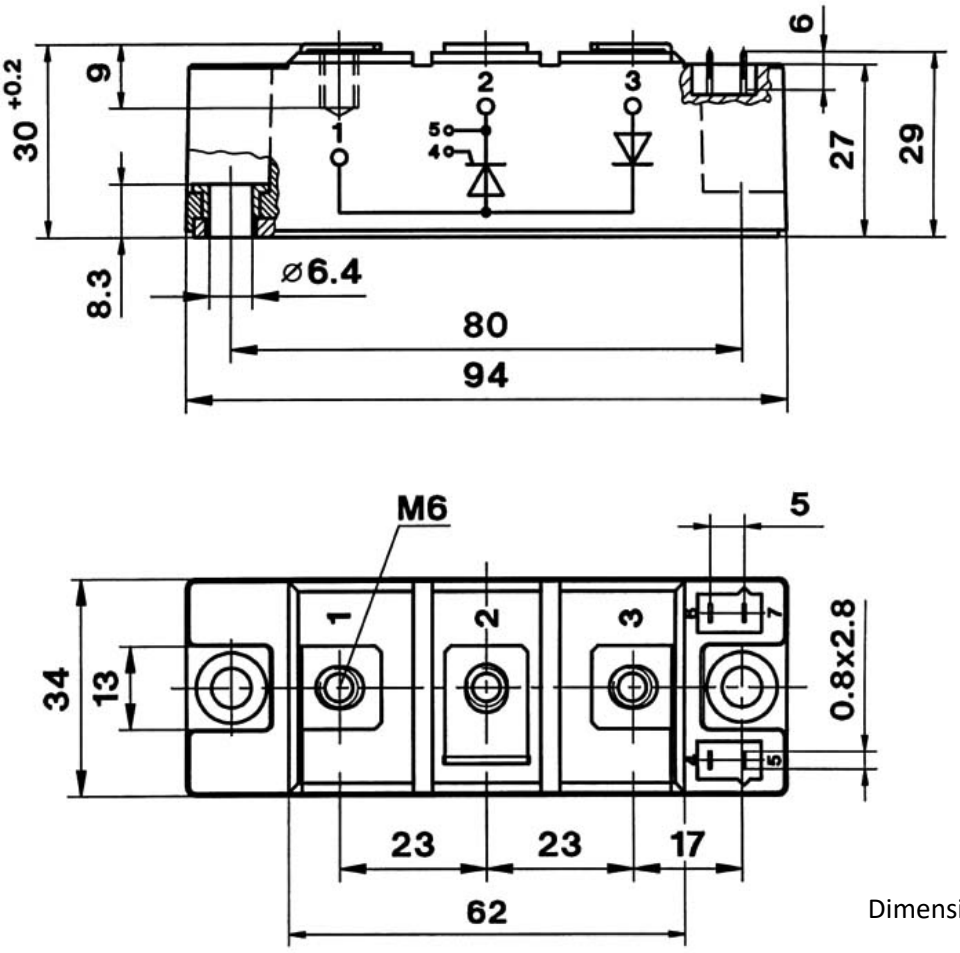


Fig. 9: Gate trigger characteristics

DIMENSIONS



Dimensions in mm

TOPOLOGY OF INTERNAL CONNECTION