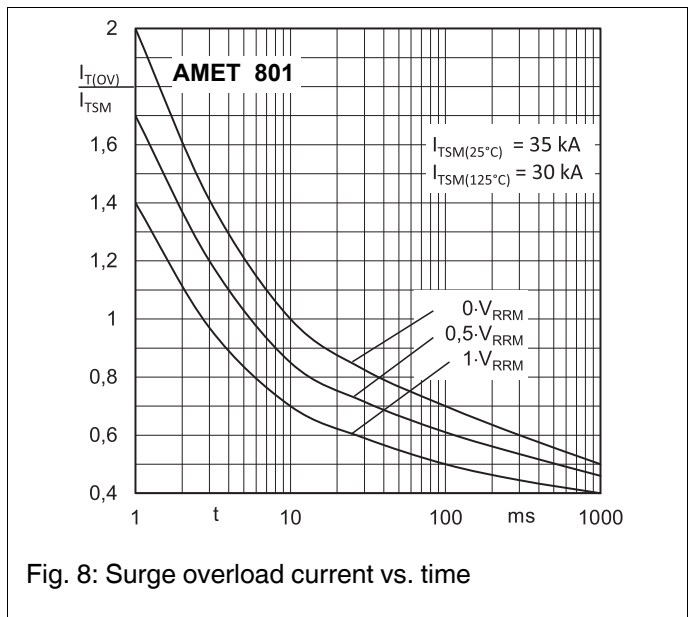
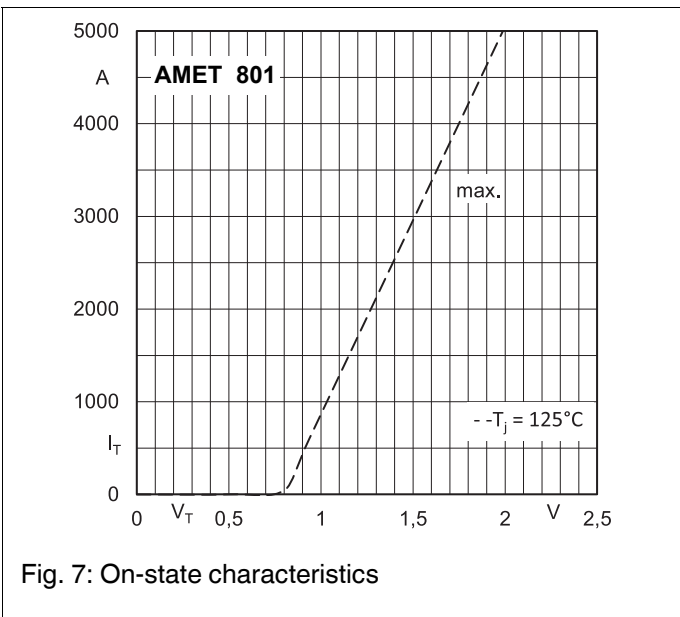
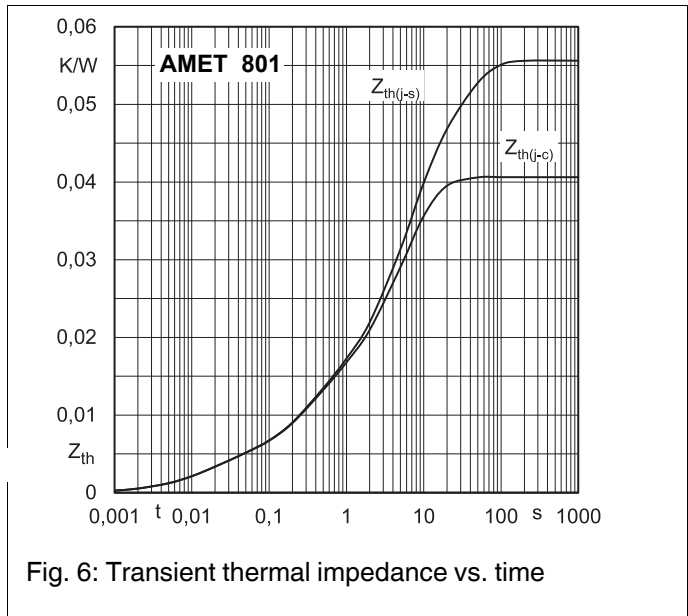
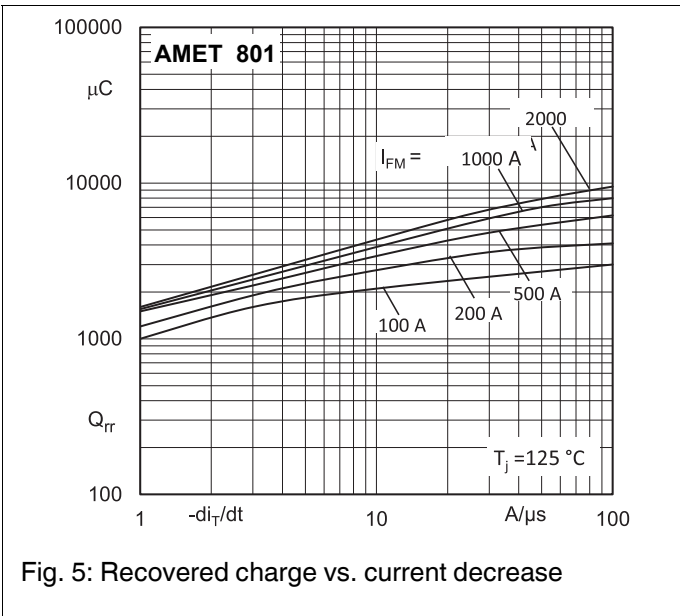
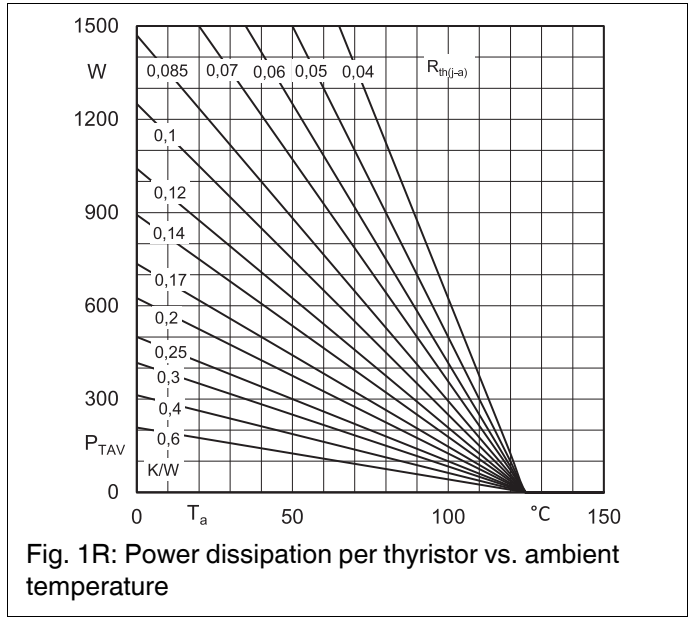
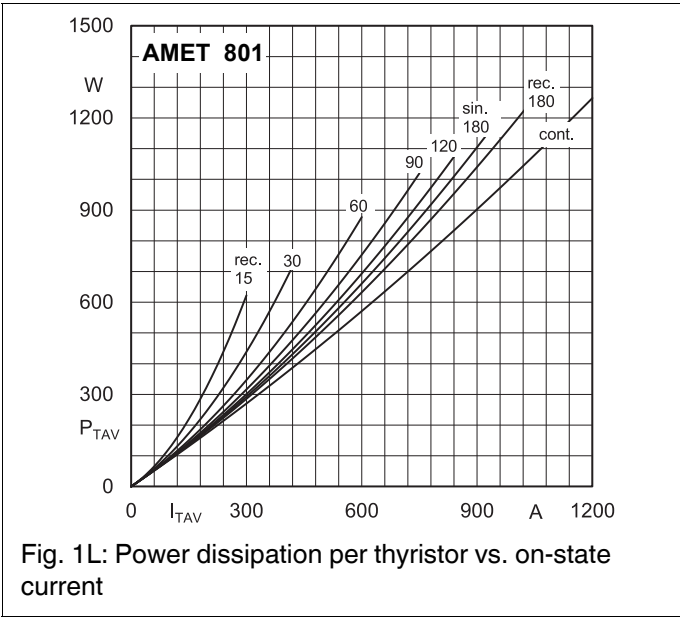




Symbols and parameters			Values	Units
$I_{T(AV)}$	Average on-state current	sin 180; $T_C = 85 (100)^\circ\text{C}$	819 (564)	A
$I_{TRMS}$	RMS on-state current	continuous operation	1500	A
$V_{RSM}$	Non-repetitive peak reverse voltage		1900	V
$V_{RRM}$	Repetitive peak reverse voltage		1800	V
$V_{DRM}$	Repetitive peak off-state voltage		1800	V
$I_{TSM}$	Surge on-state current	$T_j = 25^\circ\text{C}; 10 \text{ ms}$	35000	A
		$T_j = 125^\circ\text{C}; 10 \text{ ms}$	30000	A
$I^2t$	$I^2t$ value, rating for fusing	$T_j = 25^\circ\text{C}; 10 \text{ ms}$	61250000	$\text{A}^2\text{s}$
		$T_j = 125^\circ\text{C}; 10 \text{ ms}$	45000000	$\text{A}^2\text{s}$
$V_T$	On-state voltage	$T_j = 125^\circ\text{C}; I_T = 3000 \text{ A}$	max. 1.51	V
$V_{T(TO)}$	On-state threshold voltage	$T_j = 125^\circ\text{C}$	max. 0.82	V
$r_T$	On-state slope resistance	$T_j = 125^\circ\text{C}$	max. 0.17	$\text{m}\Omega$
$I_{DD}; I_{RD}$	Forward off-state current; Direct reverse current	$T_j = 125^\circ\text{C}, V_{RD} = V_{RRM}; V_{DD} = V_{DRM}$	max. 150	mA
$t_{gd}$	Gate controlled turn-on delay time	$T_j = 25^\circ\text{C}; I_G = 1 \text{ A}; di_G/dt = 1 \text{ A}/\mu\text{s}$	max. 4	$\mu\text{s}$
$(di/dt)_{cr}$	Critical rate of rise of on-state current		200	$\text{A}/\mu\text{s}$
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage		1000	$\text{V}/\mu\text{s}$
$t_q$	Turn-off time		typ. 240	$\mu\text{s}$
$I_H$	Holding current	$T_j = 25^\circ\text{C}$	max. 500	mA
$I_L$	Latching current	$T_j = 25^\circ\text{C}; R_G = 33 \Omega$	max. 2500	mA
$V_{GT}$	Gate trigger voltage	$T_j = 25^\circ\text{C}; \text{d.c.}$	min. 2	V
$I_{GT}$	Gate trigger current	$T_j = 25^\circ\text{C}; \text{d.c.}$	min. 250	mA
$V_{GD}$	Gate non-trigger voltage	$T_j = 125^\circ\text{C}; \text{d.c.}$	max. 0.2	V
$I_{GD}$	Gate non-trigger current	$T_j = 125^\circ\text{C}; \text{d.c.}$	max. 10	mA
$R_{th(j-c)}$	Thermal resistance, junction to case	cont.; per chip / per module	0.0405	K/W
		sin.180; per chip / per module	0.042	K/W
		rec.120; per chip / per module	0.043	K/W
$R_{th(c-s)}$	Thermal resistance, junction to heatsink	per chip / per module	0.015	K/W
$T_j$	Junction temperature		-40 ... +125	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		-40 ... +130	$^\circ\text{C}$
$V_{isol}$	Insulation test voltage (r.m.s.)	a.c. 50 Hz; r.m.s.; 1s / 1min.	3600 / 3000	$\text{V}\sim$
$M_s$	Mounting torque on heatsink	min. / max	5.1 / 6.9	Nm
$M_t$	Mounting torque for terminals	min. / max	16.2 / 19.8	Nm
$a$	Maximum allowable acceleration		5*9.81	$\text{m}/\text{s}^2$
$W$	Weight	approx.	1950	g



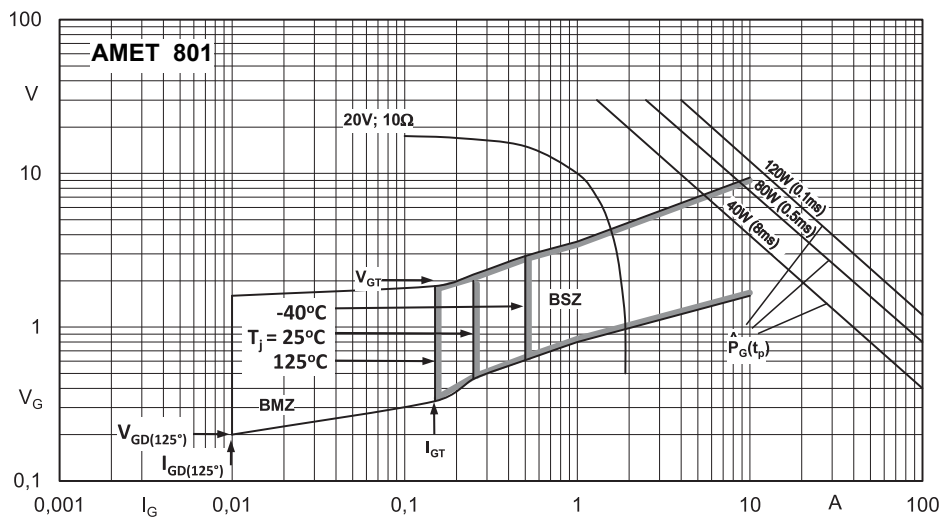
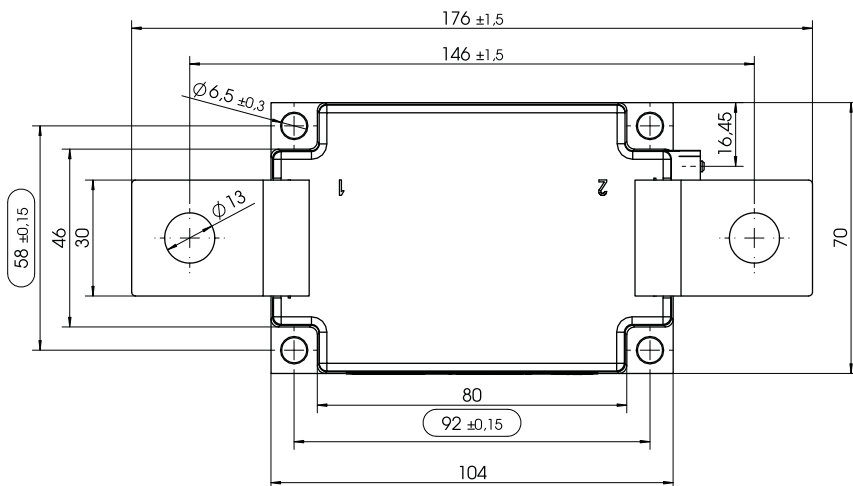
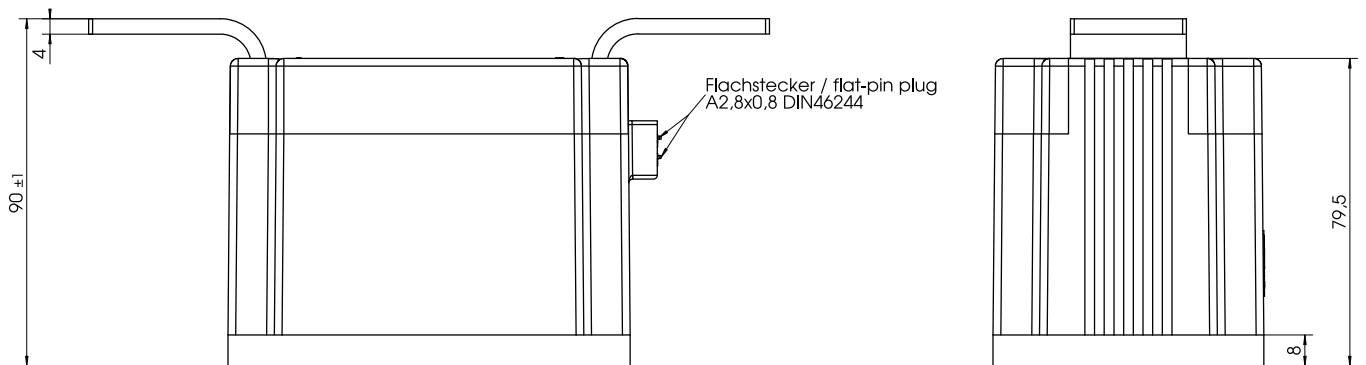


Fig. 9: Gate trigger characteristics

### DIMENSIONS



Dimensions in mm  
General tolerance ± 0.5 mm

### TOPOLOGY OF INTERNAL CONNECTION

