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HIGH CURRENT PHASE CONTROL
THYRISTOR INSULATED MODULE

AZT805

Repetitive voltage up to	**1800 V**
Mean forward current	**819 A**
Surge current	**30 kA**

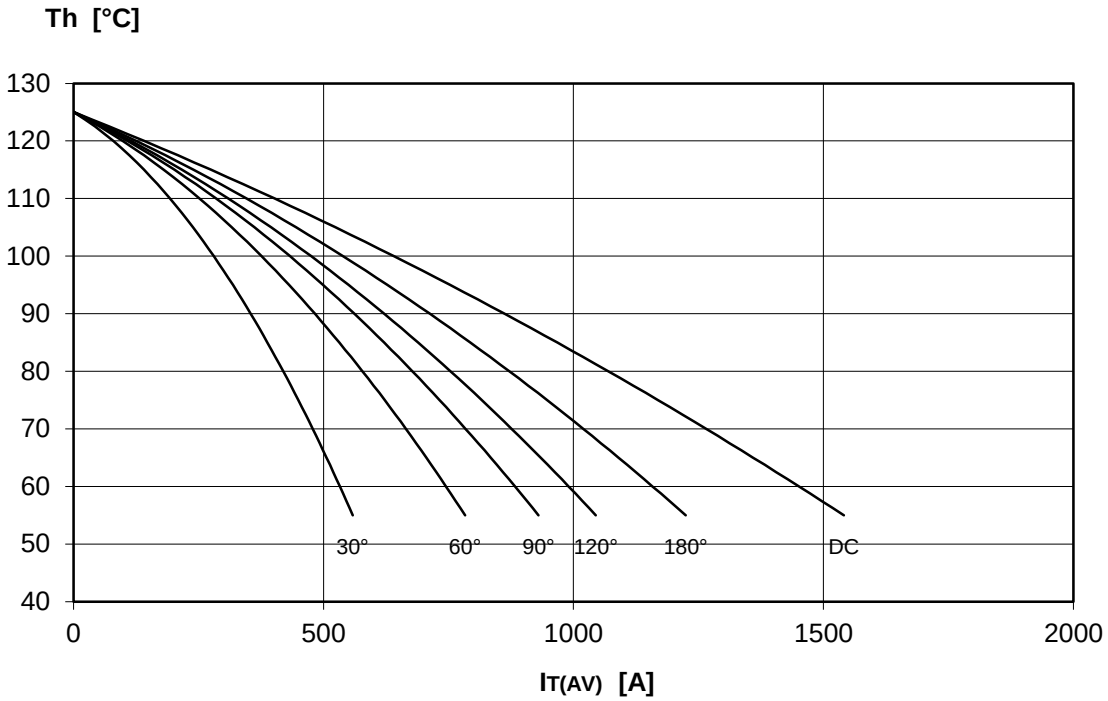
FINAL SPECIFICATION
Oct. 18 - Issue: 0

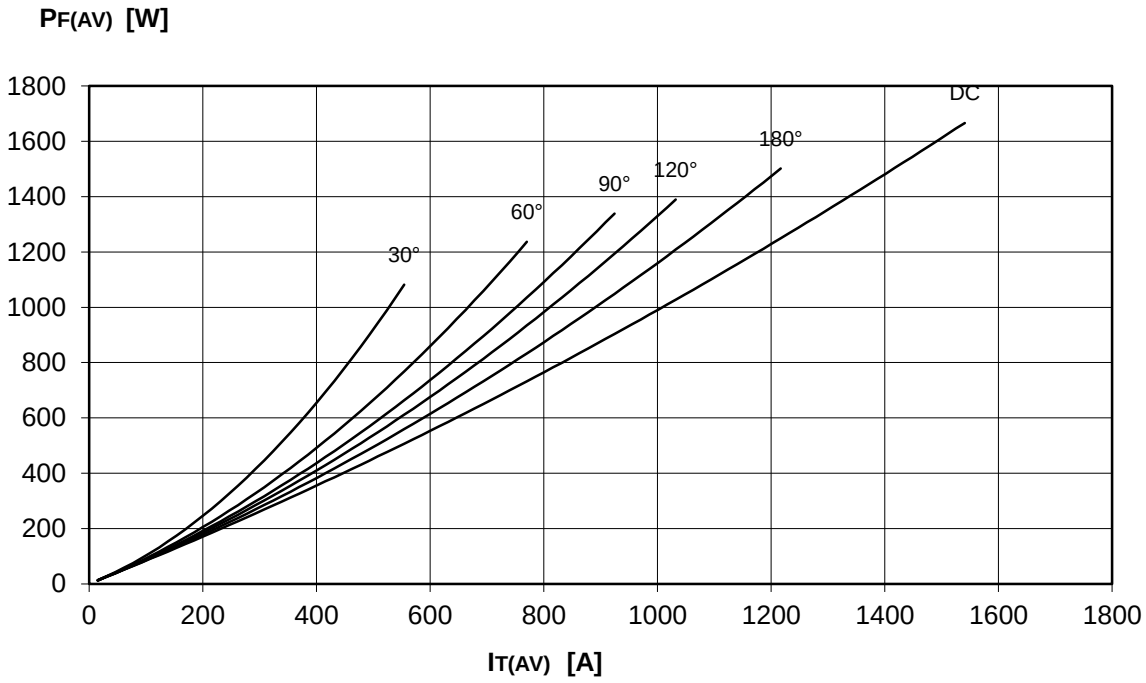
Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	1800	V
V_{RSM}	Non-repetitive peak reverse voltage		125	1900	V
V_{DRM}	Repetitive peak off-state voltage		125	1800	V
I_{RRM}	Repetitive peak reverse current		125	70	mA
I_{DRM}	Repetitive peak off-state current		125	70	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Tc=55°C, double side cooled		1243	A
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Tc=85°C, double side cooled		819	A
I_{TSM}	Surge forward current	Sine wave, 10 ms without reverse voltage	125	30	kA
I^2t	I^2t			4500 x 10^3	A^2s
V_T	On-state voltage	On-state current = 3000 A	25	1,51	V
$V_{T(TO)}$	Threshold voltage		125	0,82	V
r_T	On-state slope resistance		125	0,170	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 1050 A; gate 10V, 5Ω	125	200	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	1000	V/µs
t_d	Gate controlled delay time, typical	VD=100V; gate source 25V, 10Ω , tr=.5 µs	25	4	µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 20 V/µs linear up to 75% VDRM	125	350	µs
Q_{rr}	Reverse recovery charge	di/dt = -20 A/µs, I= 700 A			µC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	500	mA
I_L	Latching current, typical	VD=5V, tp=30µs	25	2500	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	2,00	V
I_{GT}	Gate trigger current	VD=5V	25	250	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,25	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-c)}$	Thermal impedance, DC	Junction to case, per element		42,0	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, per element		20	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
V_{ins}	RMS insulation voltage	50 hz , circuit to base, all terminal shorted	25	3000	V
T	Mounting torque	Case to heatsink		4,0 / 6,0	kN
		Busbars to terminals		12,0 / 18,0	kN
	Mass			1950	g

ORDERING INFORMATION : AZT805 S 18
standard specification — VRRM/100

DISSIPATION CHARACTERISTICS

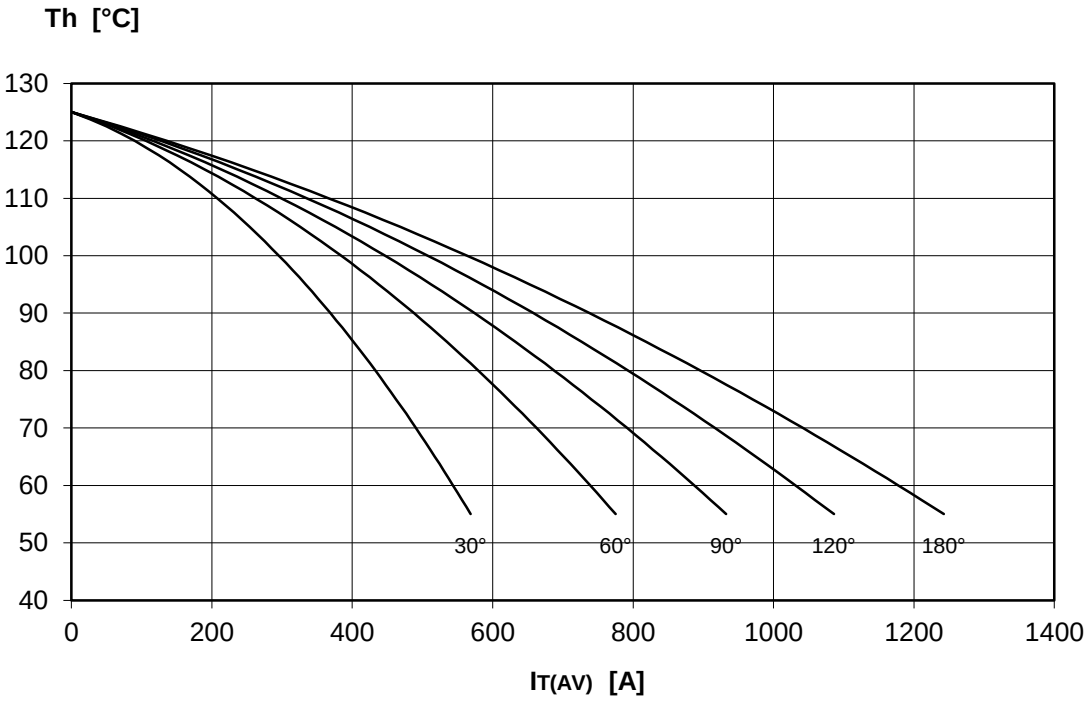
SQUARE WAVE

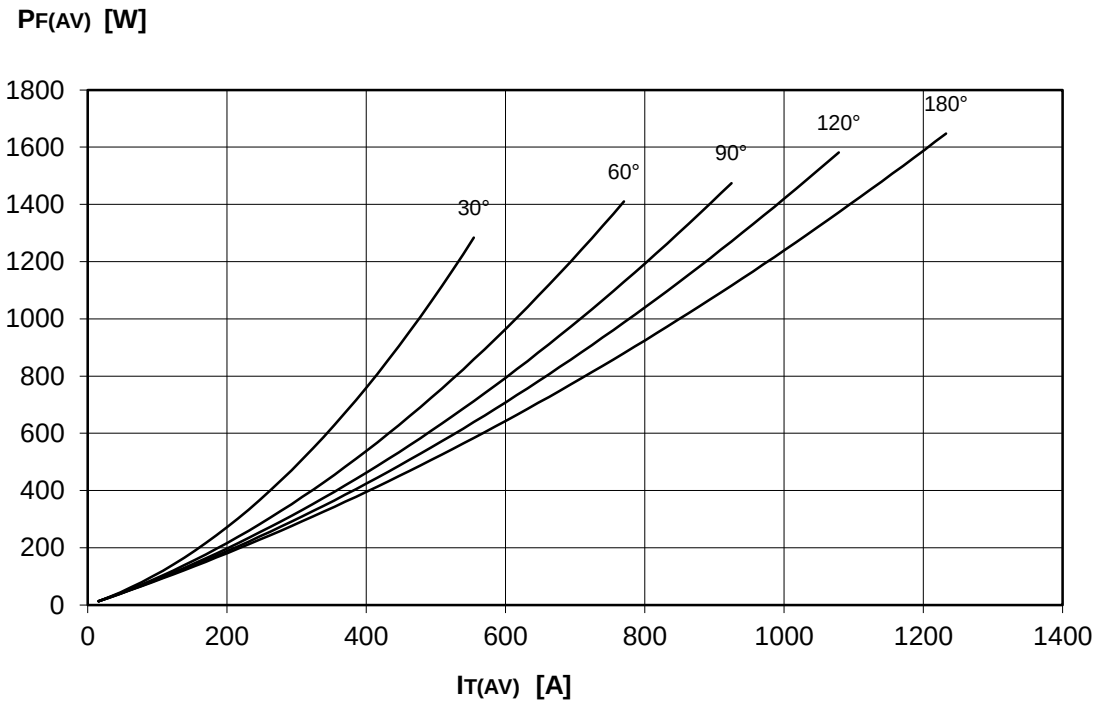




DISSIPATION CHARACTERISTICS

SINE WAVE

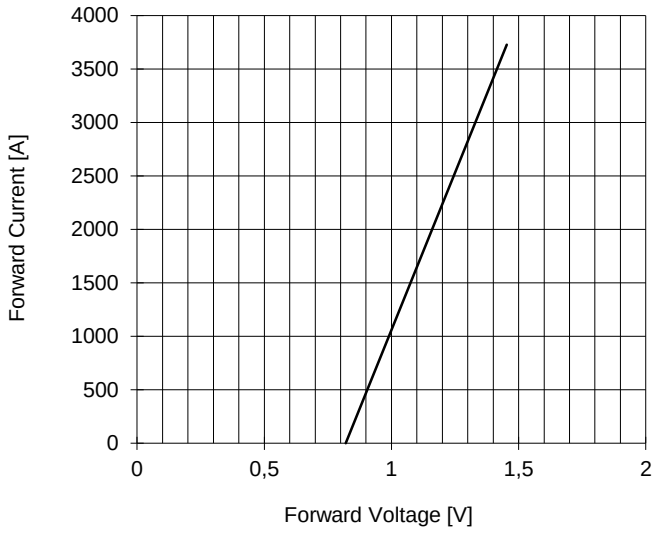




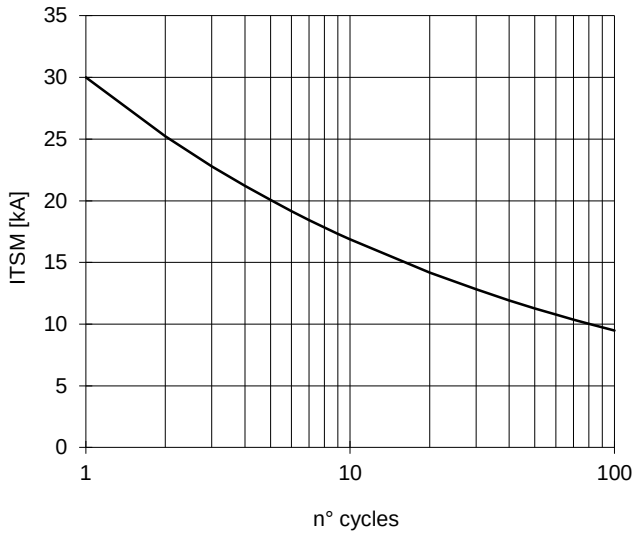
AZT805 HIGH CURRENT PHASE CONTROL

FINAL SPECIFICATION Oct. 18 - Issue: 0

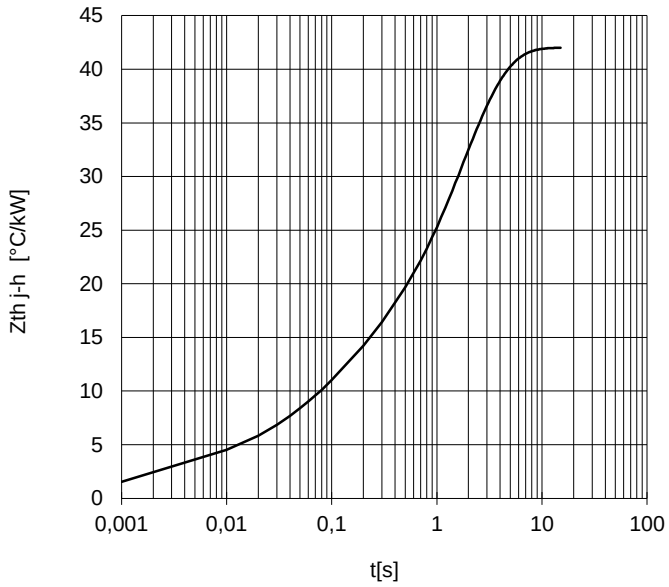
FORWARD CHARACTERISTIC
Tj = 125 °C

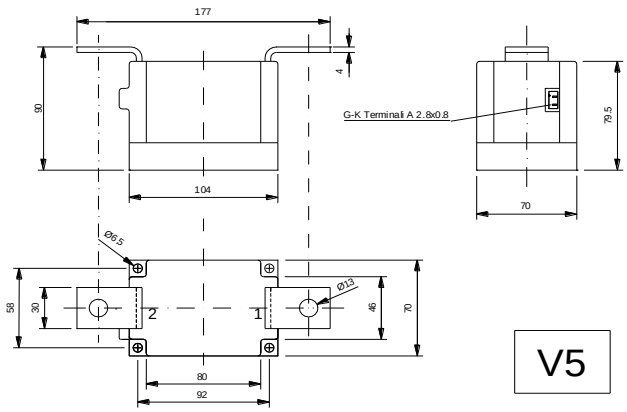


SURGE CHARACTERISTIC
Tj = 125 °C

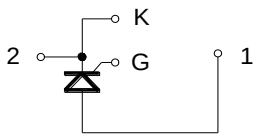


TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





V5



All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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