POLOVODIČE
akciová společnost

TG 919-1400-45

Gate Turn-off Thyristor

Properties

- Full reverse voltage
- High reliability
- Suitable for drives and traction applications

Key Parameters

V_{DRM}, V_{RRM}	=	4 500	V
I_{TGQM}	=	1 400	A
I_{TAVm}	=	600	A
I_{TSM}	=	12 000	A
V_{TO}	=	2.306	V
r_T	=	1.301	mΩ

Types

	V_{DRM}, V_{RRM}
TG 919-1400-45	**4 500 V**
TG 919-1400-40	**4 000 V**
TG 919-1400-36	**3 600 V**
Conditions:	T_j = -40 ÷ 115 °C, half sine waveform, f = 50Hz

Mechanical Data

F_m	**Mounting force**	15 ± 3	kN
m	**Weight**	0.82	kg
D_S	**Surface creepage distance**	25	mm
D_a	**Air strike distance**	13	mm

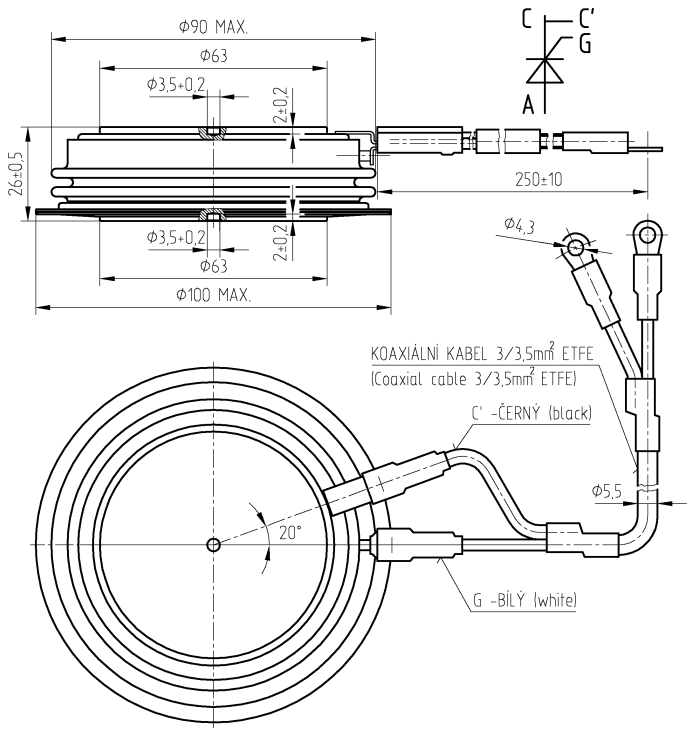

Fig. 1 Case

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Maximum Ratings			*Maximum Limits*	*Unit*
V_{DRM} V_{RRM}	**Repetitive peak off-state and peak reverse voltage** T_j = -40 ÷ 115 ℃, V_{GC} = -2 V	**TG 919-1400-45** **TG 919-1400-40** **TG 919-1400-36**	**4 500** **4 000** **3 600**	**V**
I_{TGQM}	**Peak Turn-off current** T_j = -40 ÷ 115 ℃, C_S = 4 µF, di_{GC}/dt = -35 A/µs, V_{DM} = 0.8 V_{DRM}		**1 400**	**A**
I_{TRMS}	**RMS on-state current** T_c = 70 ℃, half sine waveform, f = 50 Hz		**940**	**A**
I_{TAVm}	**Average on-state current** T_c = 70 ℃, half sine waveform, f = 50 Hz		**600**	**A**
I_{TSM}	**Peak non-repetitive surge** half sine pulse, t_p = 10 ms, V_R = 0 V		**12 000**	**A**
I^2t	**Limiting load integral** half sine pulse, t_p = 10 ms, V_R = 0 V		**720 000**	**A^2s**
$(di_T/dt)_{cr}$	**Critical rate of rise of on-state current** $I_T = I_{TGQM}$, V_D = 2/3 V_{DRM}, f = 50 Hz		**400**	**A/µs**
$(dv_D/dt)_{cr}$	**Critical rate of rise of off-state voltage** V_D = 2/3 V_{DRM}, V_{GC} = - 2 V		**1 000**	**V/µs**
V_{DSP}	**Peak turn-off voltage spike due to snubber**		**500**	**V**
I_{FGCM}	**Peak forward gate current**		**80**	**A**
I_{GCMS}	**RMS gate current**		**63**	**A**
V_{GCM}	**Peak reverse gate voltage**		**-16**	**V**
$t_{on(min)}$	**Minimum permissible on-time**		**50**	**µs**
$t_{off(min)}$	**Minimum permissible off-time**		**100**	**µs**
T_{jmin} - T_{jmax}	**Operating temperature range**		**-40 ÷ 115**	**℃**
T_{stgmin} - T_{stgmax}	**Storage temperature range**		**-40 ÷ 115**	**℃**

Unless otherwise specified T_j = 115 ℃

Type of GTO Thyristor	***Recommended Diodes***	
	SNUBBER	**FREEWHEEL**
TG 919-1400-45	**DM 827-500-45**	**DM 827-500-45**
TG 919-1400-40	**DM 827-500-40**	**DM 827-500-40**
TG 919-1400-36	**DM 827-500-36**	**DM 827-500-36**

Characteristics				Value			Unit
				min.	typ.	max.	
V_{TM}	**Maximum peak on-state voltage** I_{GT} = 2 A, I_{TM} = 1 400 A					4.200	V
V_{T0} r_T	**Threshold voltage** **Slope resistance** I_{T1} = 667 A, I_{T2} = 2 000 A					2.306 1.301	V mΩ
I_L	**Latching current** T_j = 25 ℃					120	A
I_{DM}	**Peak off-state current** $V_D = V_{DRM}$, V_{GC} = -2 V					150	mA
I_{RM}	**Peak reverse current** $V_R = V_{RRM}$					150	mA
I_{GCM}	**Peak negative gate leakage current** V_{GC} = -16 V					50	mA
V_{GT}	**Gate trigger voltage** T_j = -40 ÷ 115 ℃					1.5	V
I_{GT}	**Gate trigger current** V_D = 12 V, R_L = 0.1 Ω		T_j = - 40 ℃ T_j = 25 ℃ T_j = 125 ℃			16 1.6 0.8	A
t_f t_S t_{gq} t_{tail}	**Fall time** **Storage time** **Turn-off time** **Tail time**	Definitions as on Fig.9 V_D = 2/3 V_{DRM}, $I_{TGQ} = I_{TGQM}$, C_S = 4 µF, V_{GC} = -15 V, di_{GC}/dt = -35 A/µs				1.5 14.5 18 30	µs

Unless otherwise specified T_j = 115 ℃

Thermal Parameters		Value	Unit
R_{thjc}	**Thermal resistance junction to case** *double side cooling*	18	K/kW
R_{thch}	**Thermal resistance case to heatsink,** *double side cooling*	6	K/kW

Transient Thermal Impedance

Analytical function for transient thermal impedance

$$Z_{thjc} = \sum_{i=1}^{5} R_i (1 - \exp(-t / \tau_i))$$

Conditions:

F_m = 15 ± 3 kN, Double side cooled

i	1	2	3	4	5
R_i (K/kW)	7.32	0.63	5.74	4.10	0.21
τ_i (s)	0.5526	0.2048	0.0913	0.0170	0.0003

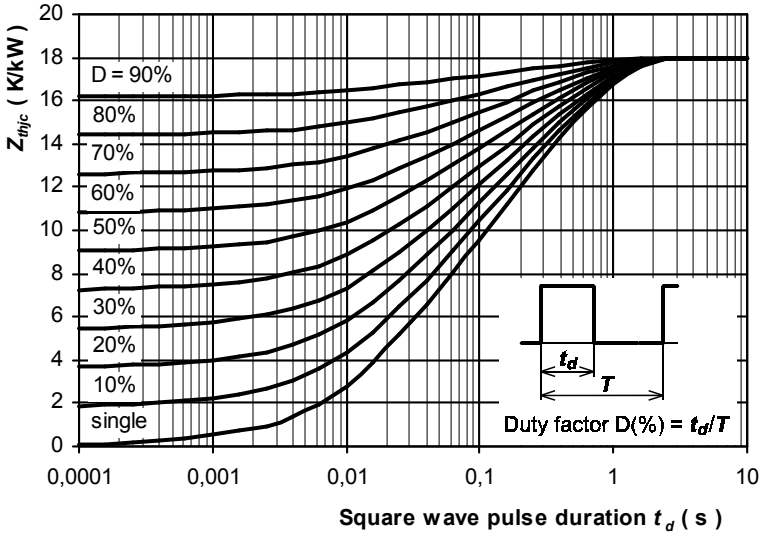

Fig.2 Transient thermal impedance junction to case (Double side cooled)

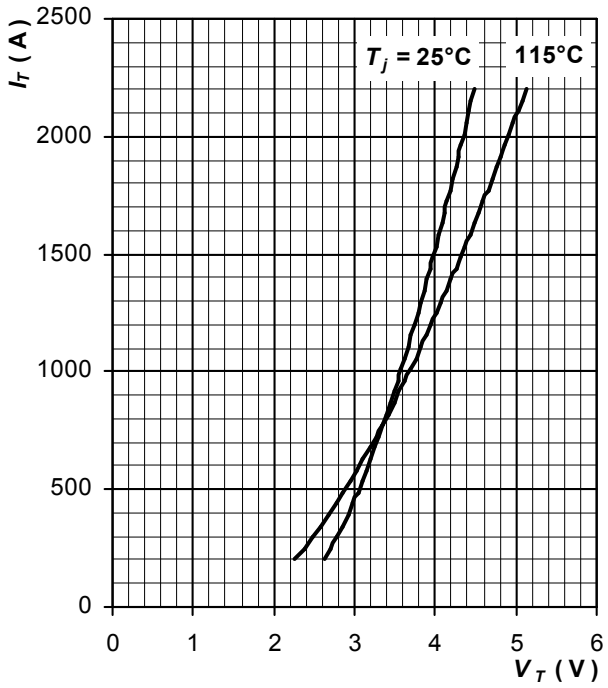

Fig.3 Maximum instaneous on-state characteristics

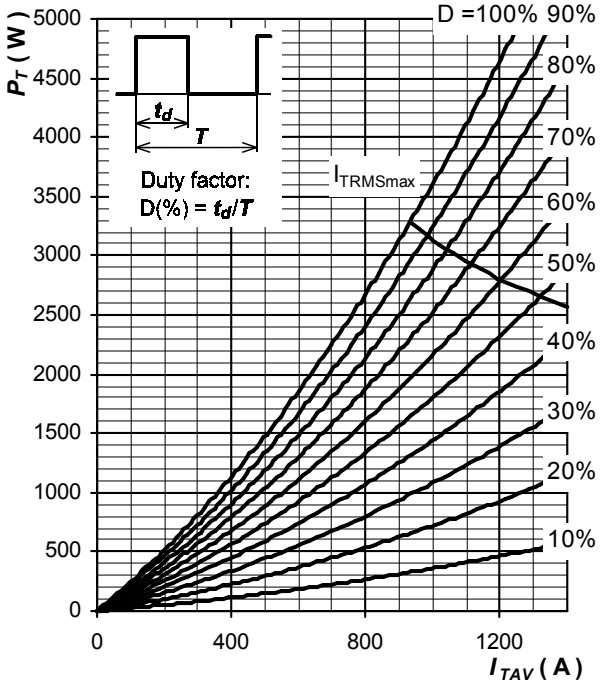

Fig.4 Power losses vs Rectangular pulse current

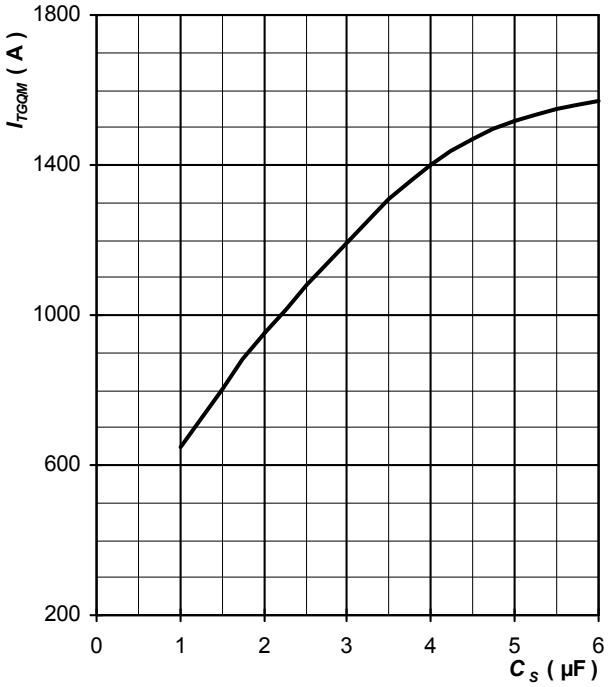

Fig.5 Maximum permissible turn-off current vs Snubber capacitance

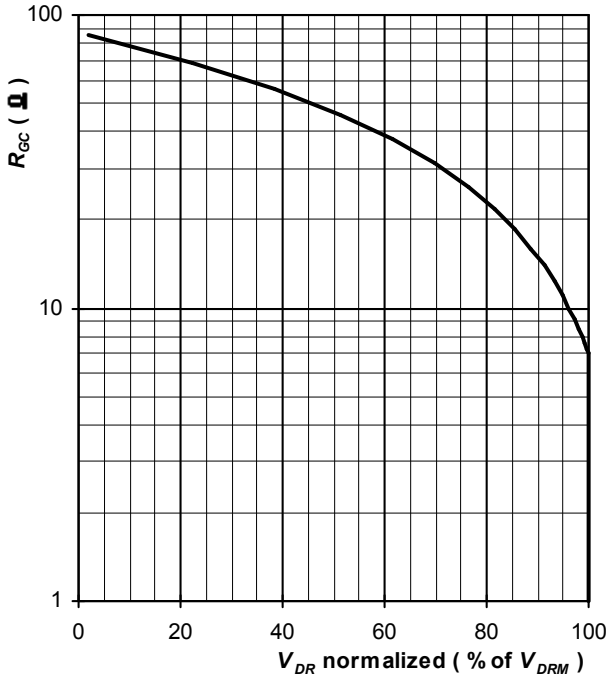

Fig.6 Maximum forward blocking voltage vs External gate-cathode resistance

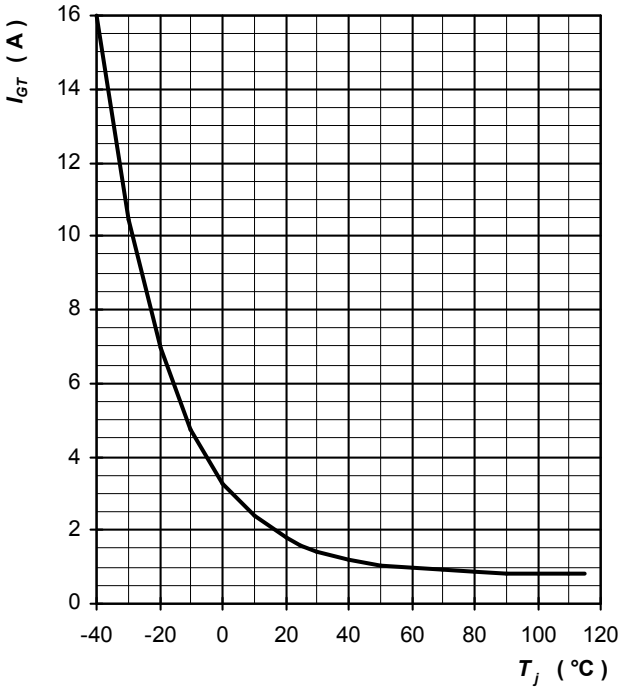

Fig.7 Maximum gate trigger current vs Junction temperature

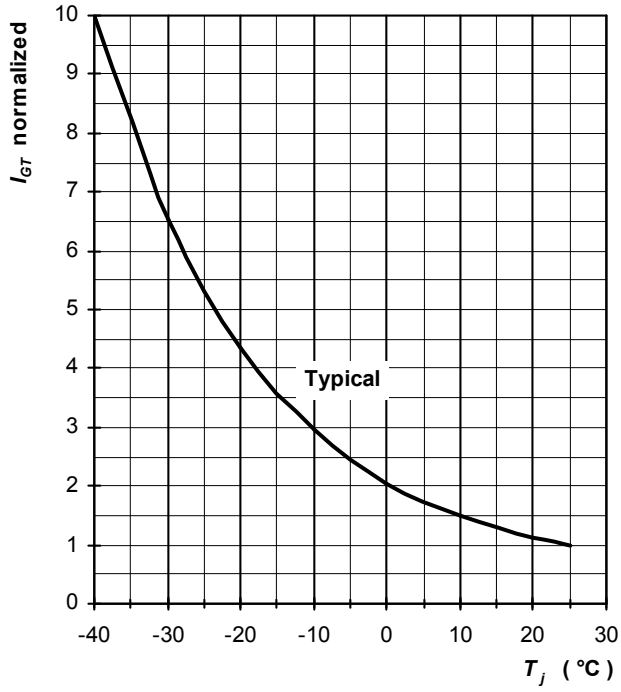

Fig.8 Gate trigger current normalized to I_{GT} by 25℃ vs Junction temperature

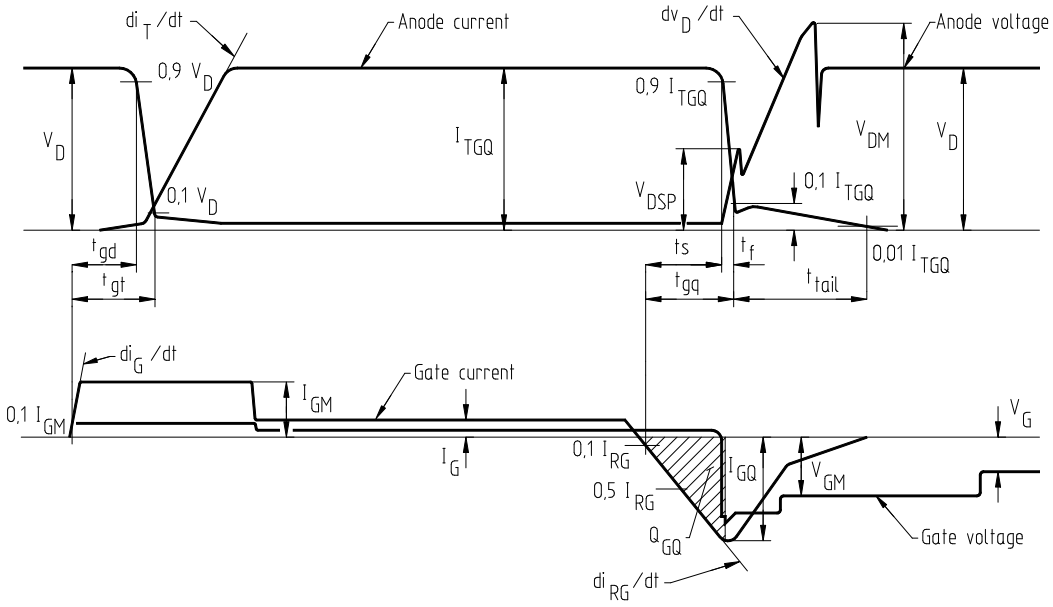

Fig.9 Turn-off waveform diagram

Notes